Digital low level RF development at Diamond Light Source

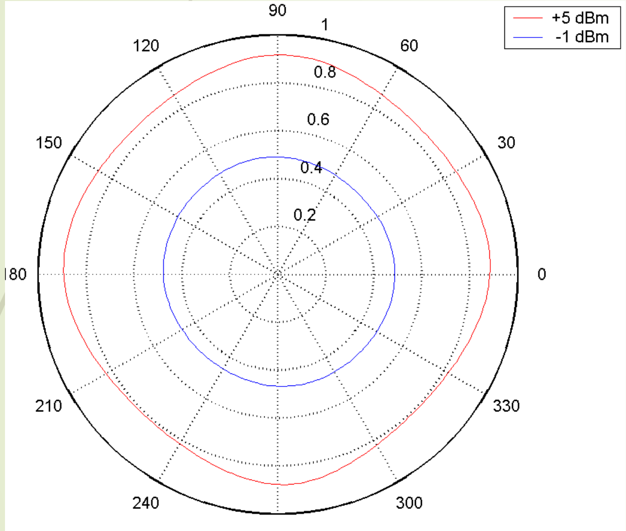
Pengda Gu RF DLS RF group

Agenda:

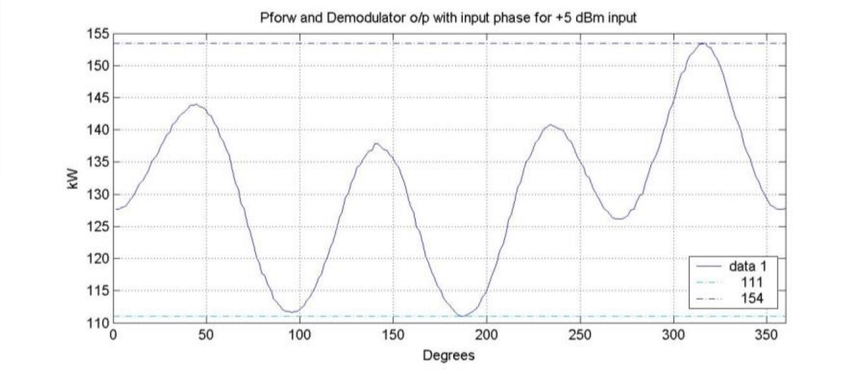
- Early start stage
- Collaboration with ALBA
- Next DLLRF for Diamond

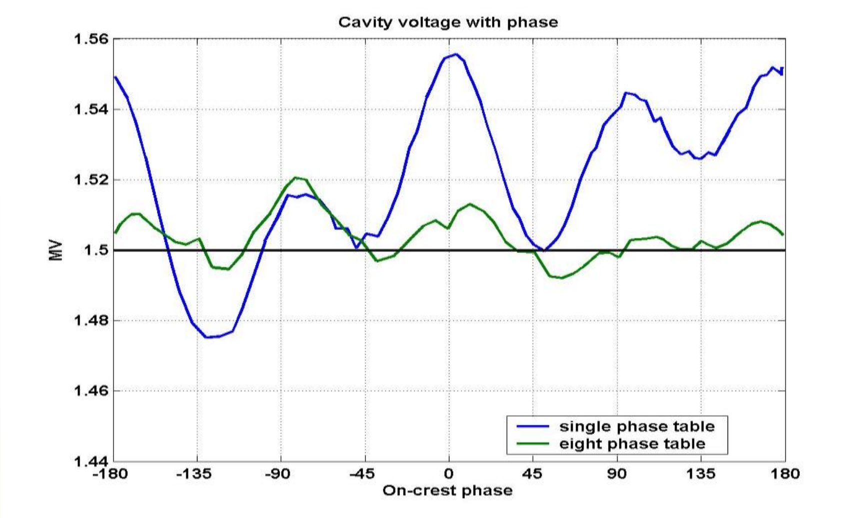
Diamond Storage Ring Analogue Low Level RF Controller

- Variation with phase of LLRF readings of Pfwd, Probe
  - Variation due to distortion in IQ demodulator
  - 8 phase lookup tables produced
  - Instability at certain phases → faulty module
  - Variation of suppression at different phases



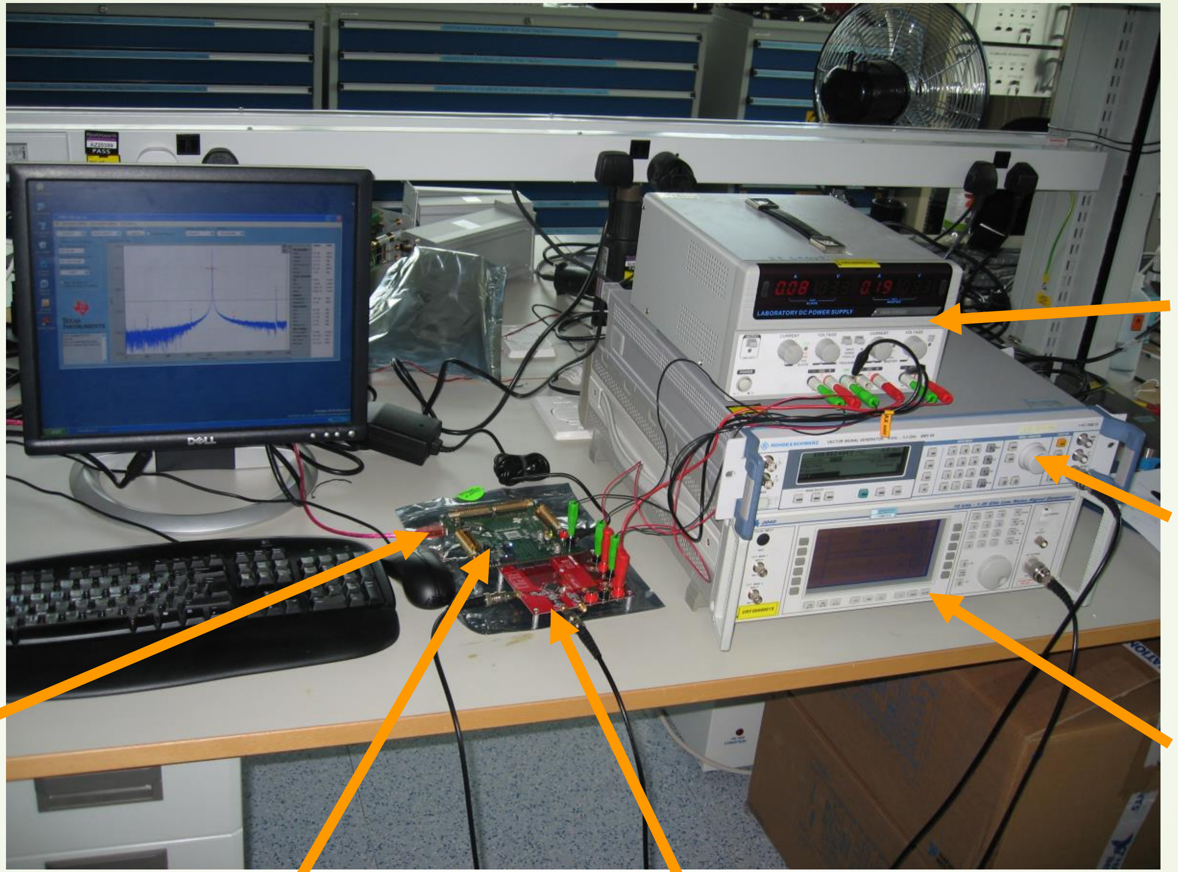
Polar plot of IQ demodulated forward power signal.
Distortion clearly visible at the higher input level.





x3 improvement from **8-point** look up table

First FPGA development



PSU

Signal generator with phase modulation

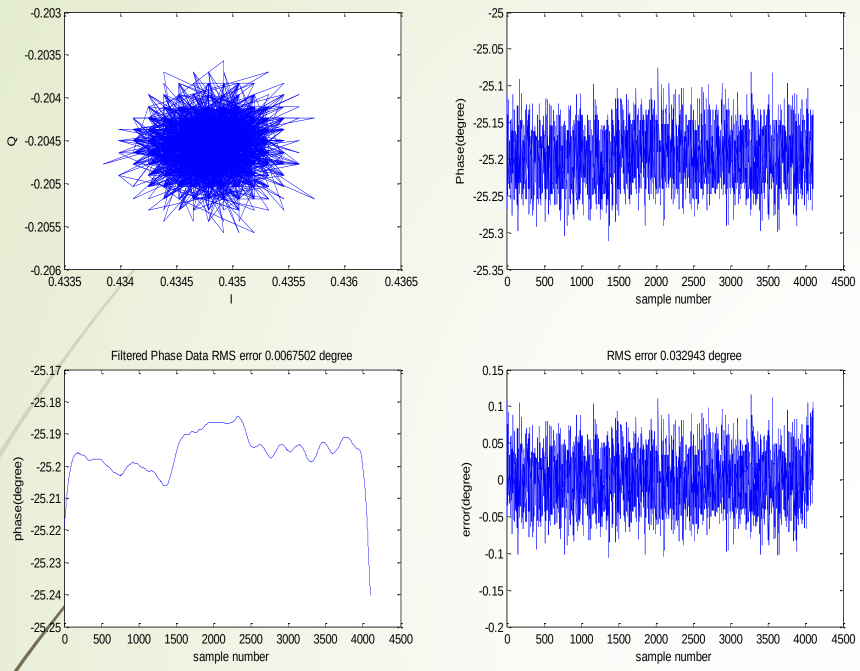
Clock signal generation

USB connection to PC

FPGA Data capture: TSW1200 by TI

ADC converter: ADS 5474 evaluation board

Raw I Q data   Calculated phase



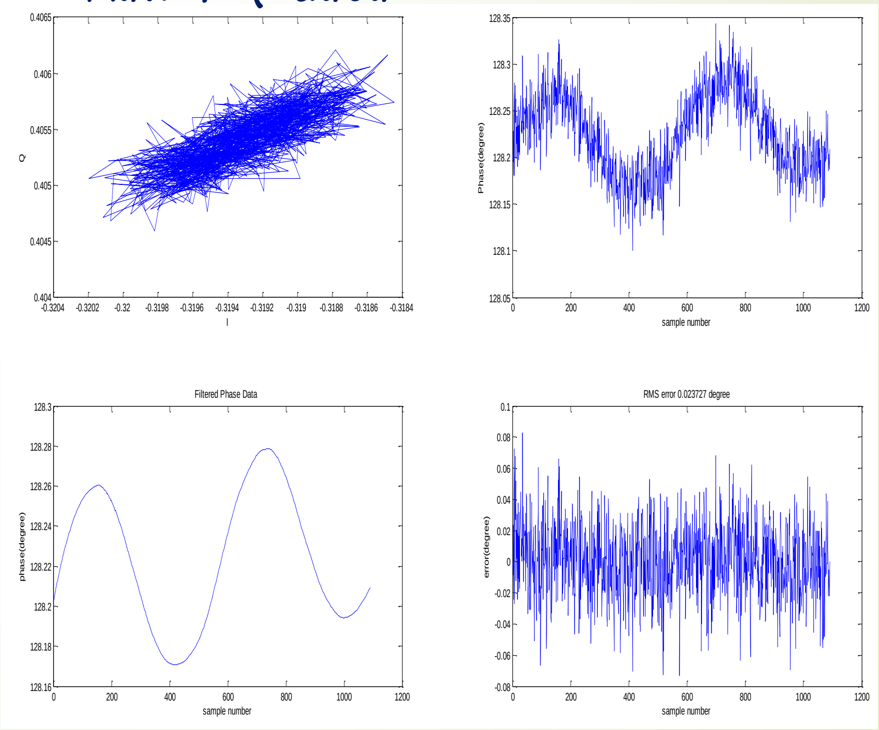
Phase calculated from

$$Mf_{IF} = Nf_{SF} \qquad \Delta\varphi = 2\pi \frac{N}{M}$$

$$I = \frac{2}{M}\sum_{i=0}^{M-1} y_i \sin(i \cdot \Delta\varphi)$$

$$Q = \frac{2}{M}\sum_{i=0}^{M-1} y_i \cos(i \cdot \Delta\varphi)$$

Raw I Q data   Calculated phase



Measurement of RF signal with 0.001 rad phase modulation

Initial phase resolution obtained is better than 0.02 deg RMS before filtering or with 0.007 deg RMS with filtering applied

Phase Measurement Unit

Two units finished and installed in RF hall.

Direct RF sampling

$$Mf_{RF} = Nf_{SF}$$

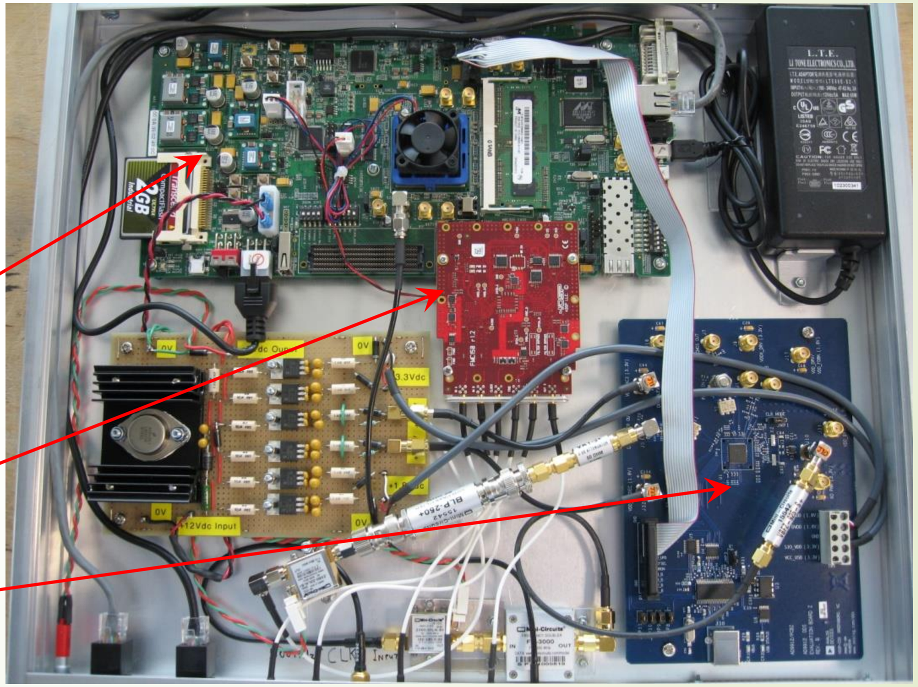
Phase advance between two samples

$$\Delta\varphi = 2\pi \frac{N}{M}$$

Then calculate I and Q

$$I = \frac{2}{M}\sum_{i=0}^{M-1} y_i \sin(i \cdot \Delta\varphi)$$

$$Q = \frac{2}{M}\sum_{i=0}^{M-1} y_i \cos(i \cdot \Delta\varphi)$$

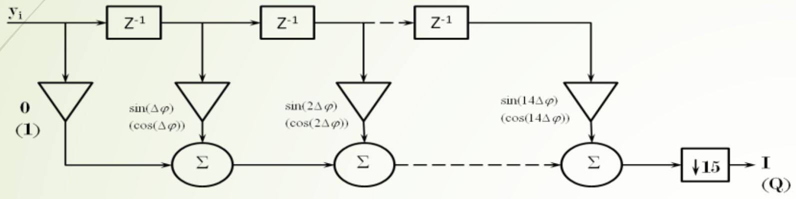


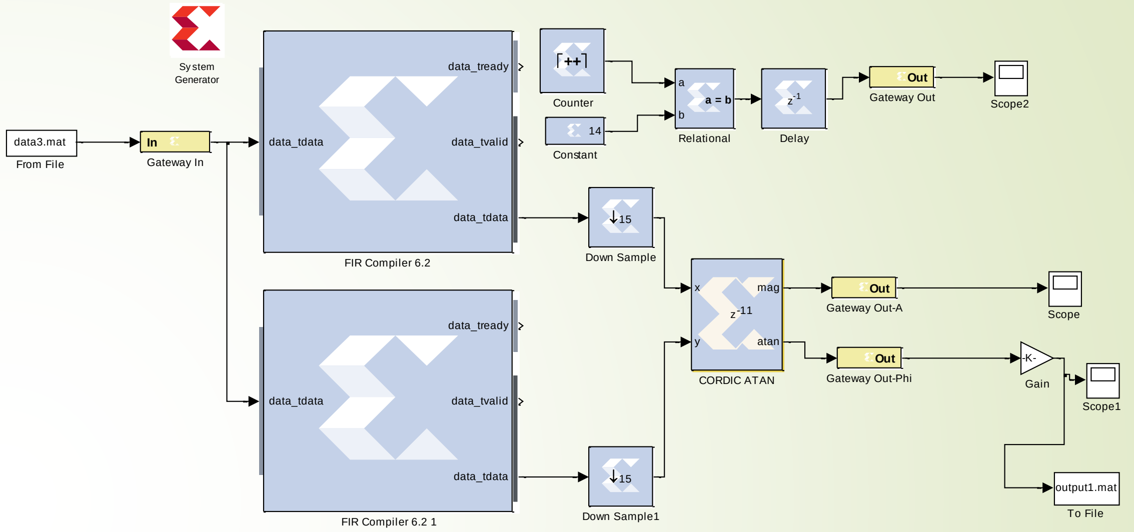
Xilinx ML605 Development Board

FMC150 module uses Texas Instruments ADS62P49 dual 14-bit, 250 MSPS ADC

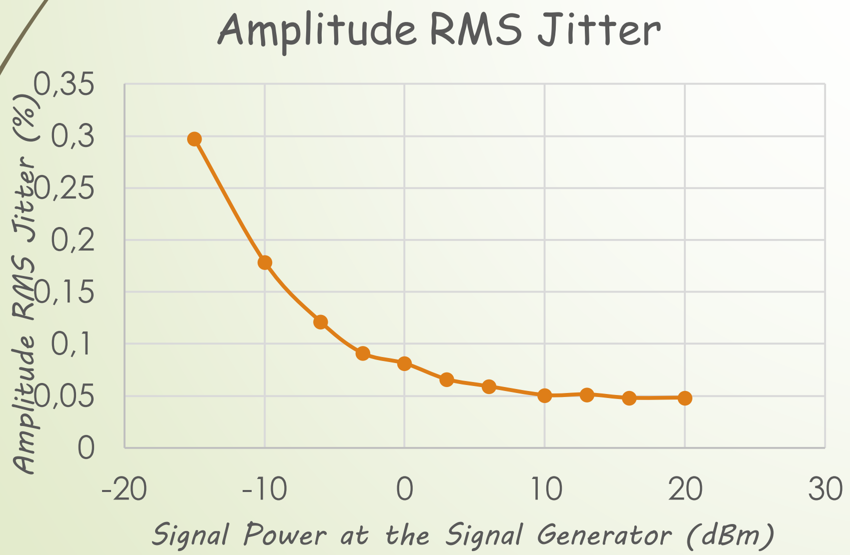
ADC clock generation constructed using ADS9912 DDS

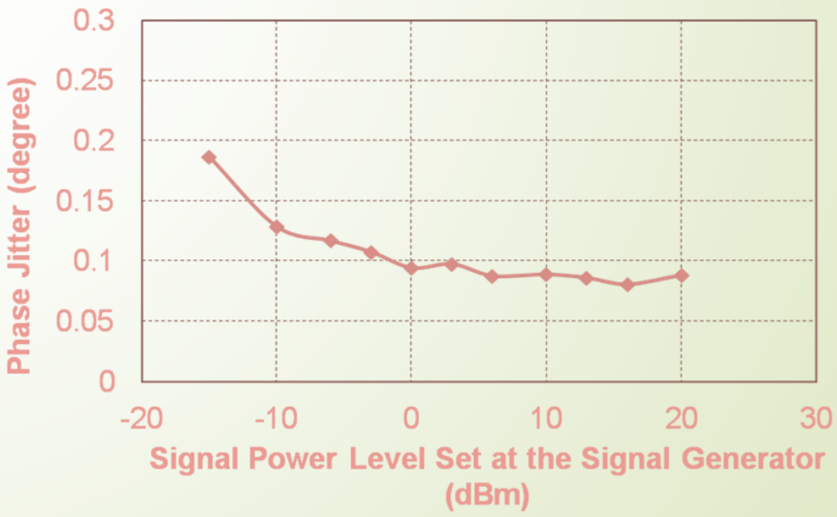
Algorithm Implementation



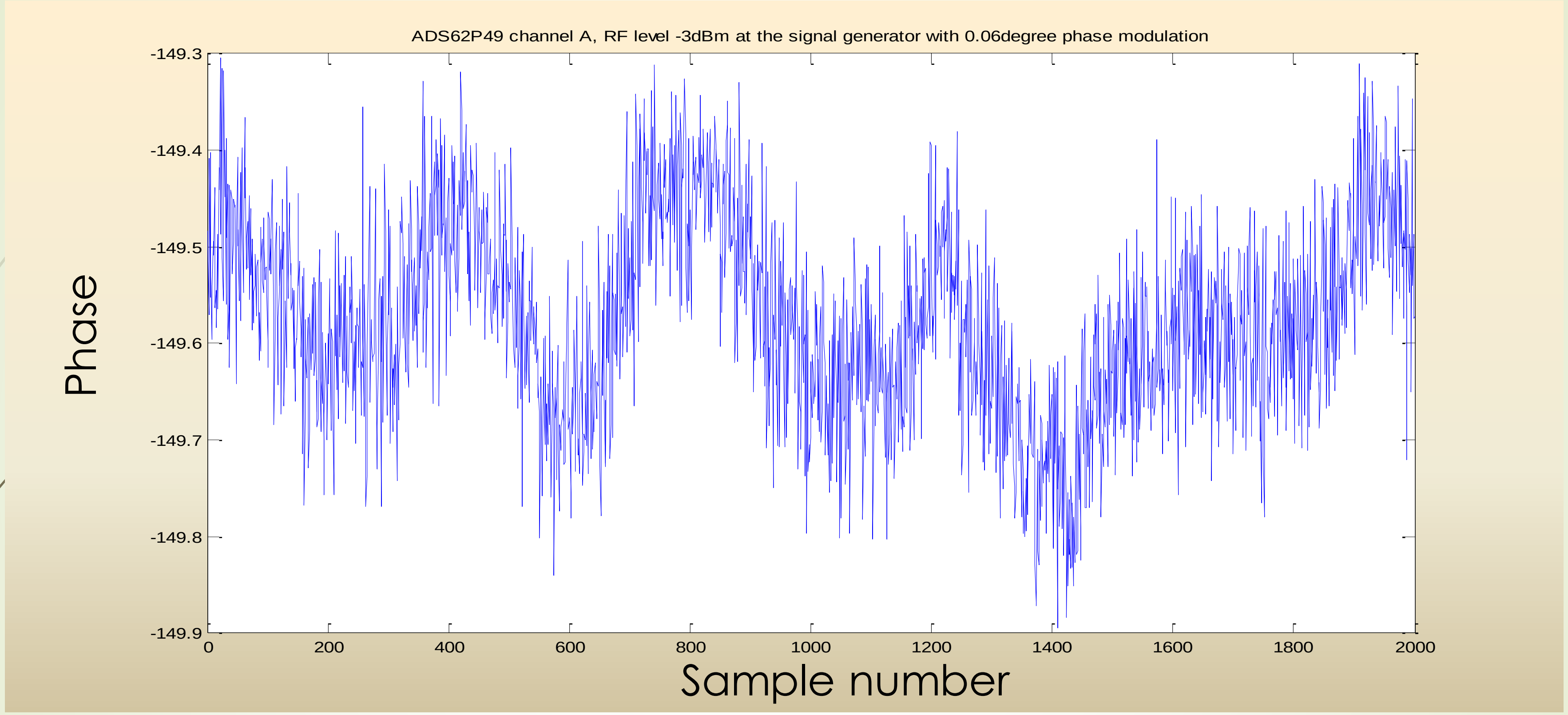


Test Results



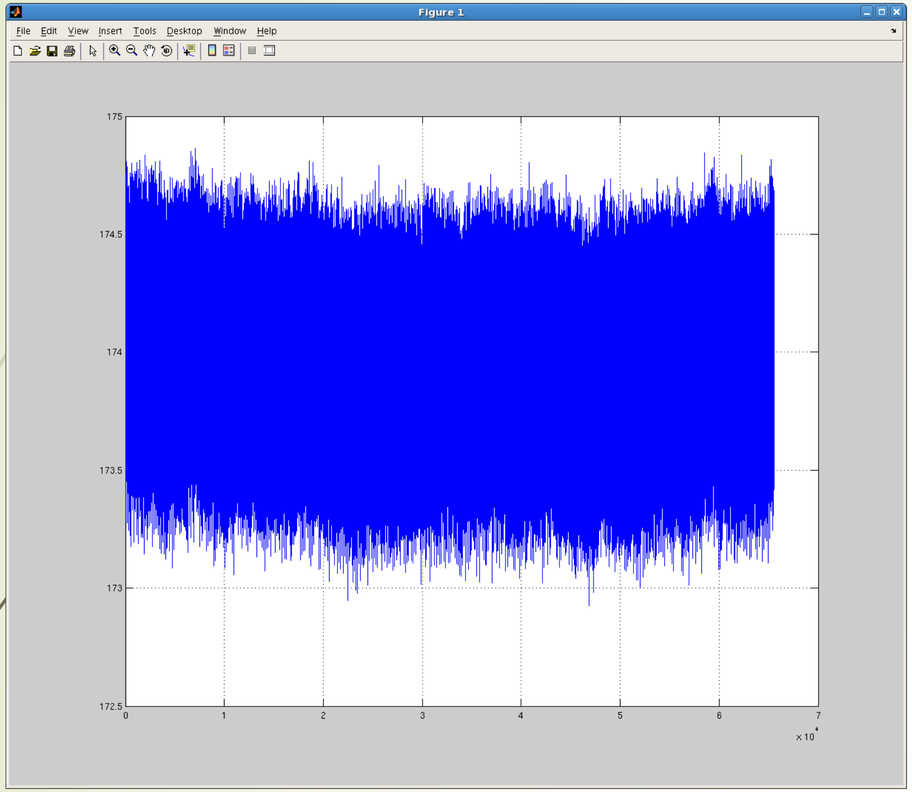


A deliberate 0.06 deg phase modulation is clearly seen from -3dBm.

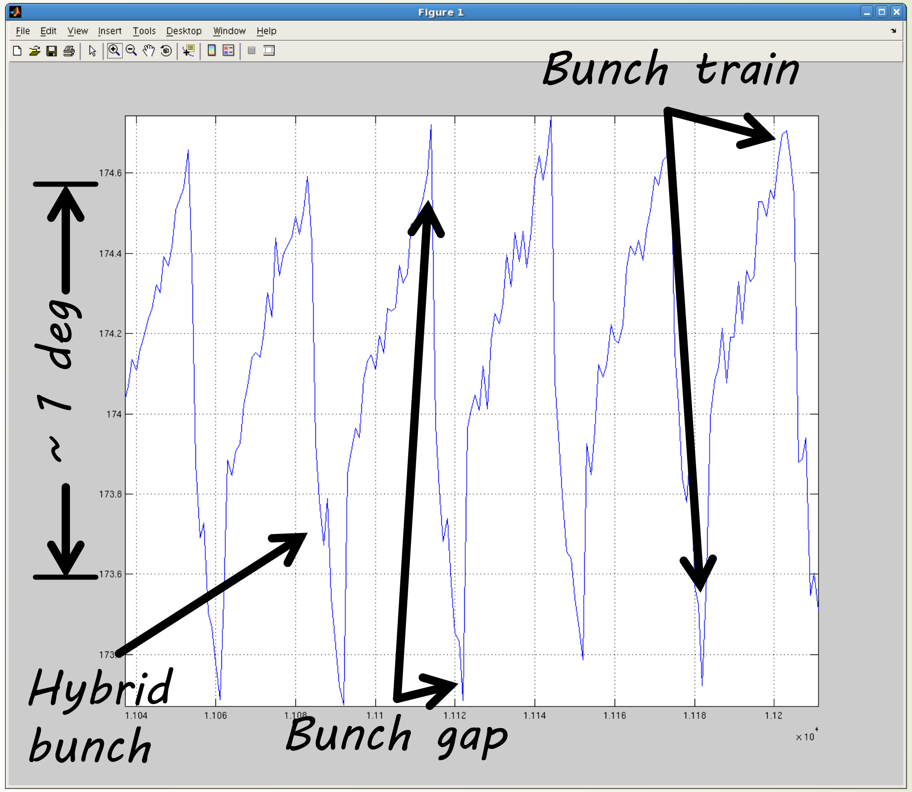


- ✓ No averaging, smoothing
- ✓ Sampling at ~ 241 MHz
- ✓ Phase measurement ~ 16 MHz

Cavity 3 Probe Signal
Phase variation and the single bunch can be clearly recognized.



Phase data



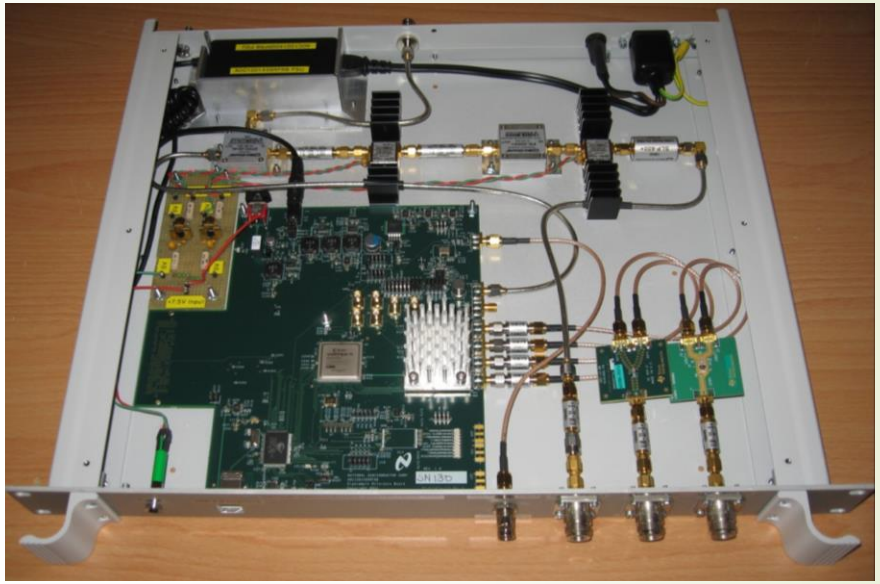
Close up shows clear phase shift across bunch train

Fast sampling and demodulation

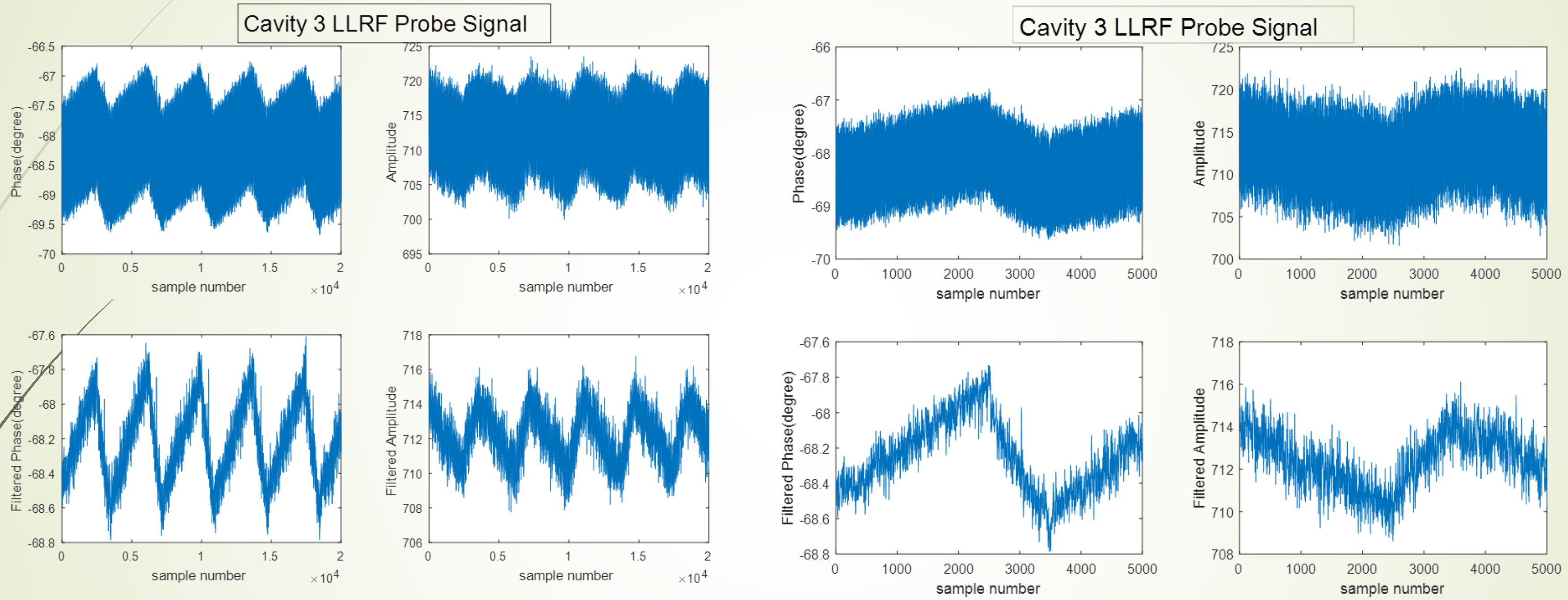
TI ADC12D1800 sampling at 2 GSPS
Sample by sample demodulation

$$\begin{pmatrix} I \\ Q \end{pmatrix} = \begin{pmatrix} \cos n\Delta\varphi & -\cos(n+1)\Delta\varphi \\ -\sin n\Delta\varphi & \sin(n+1)\Delta\varphi \end{pmatrix} \bullet \begin{pmatrix} y_{n+1} \\ y_n \end{pmatrix}$$

$$\Delta\varphi = 90^0$$

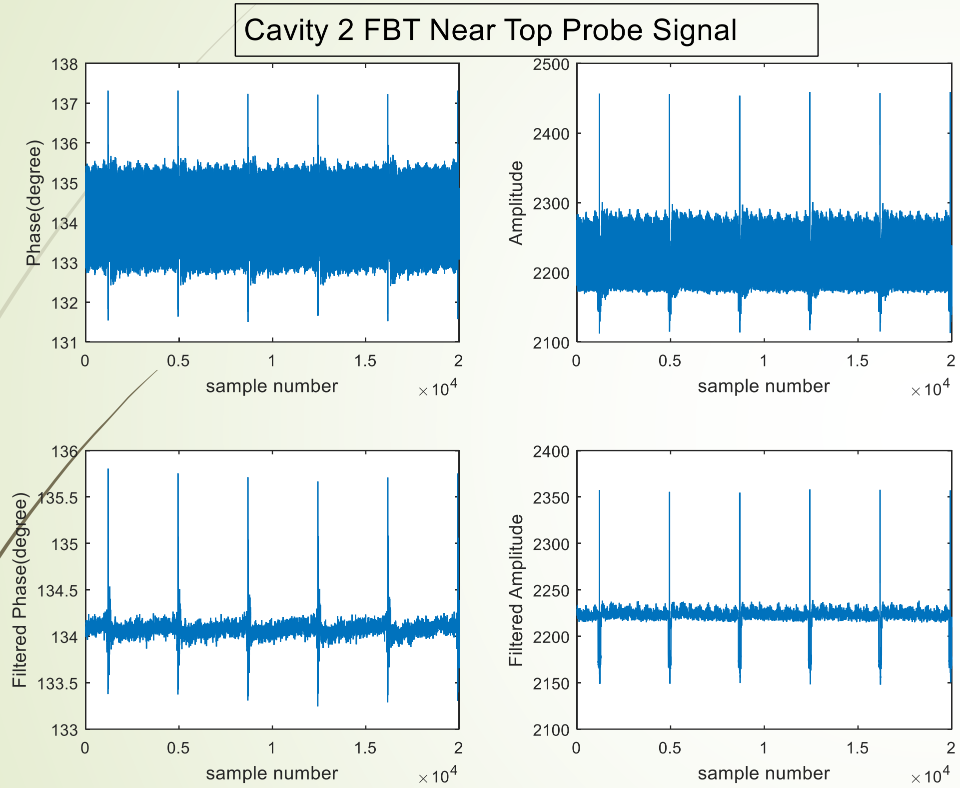


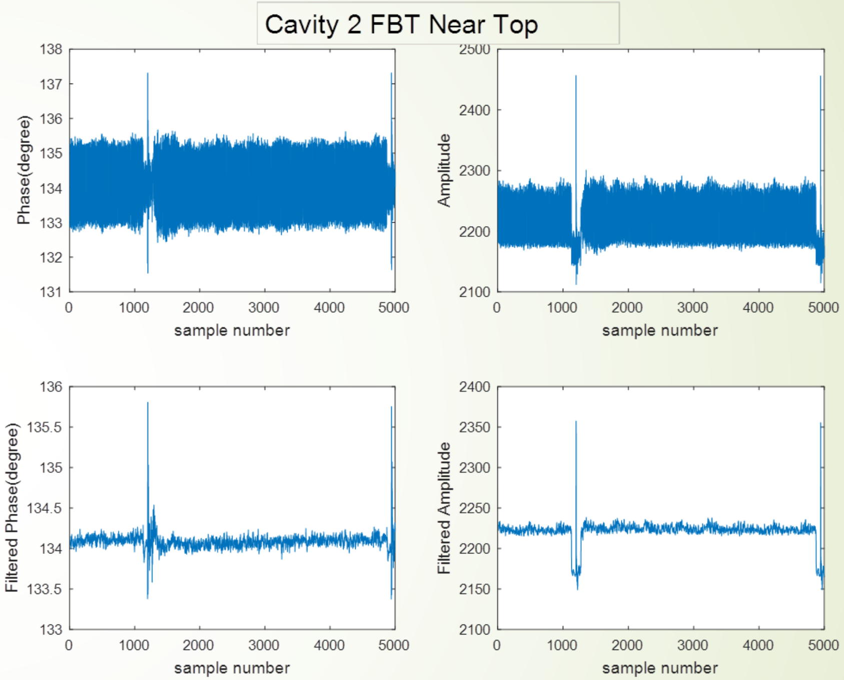
Test during normal Operation



Transient of RF field can be seen clearly.
Phase variation can clearly be observed.
Beam loading can clearly be observed.
The single bunch in the gap can clearly be observed.

Signal from the Probe at FBT

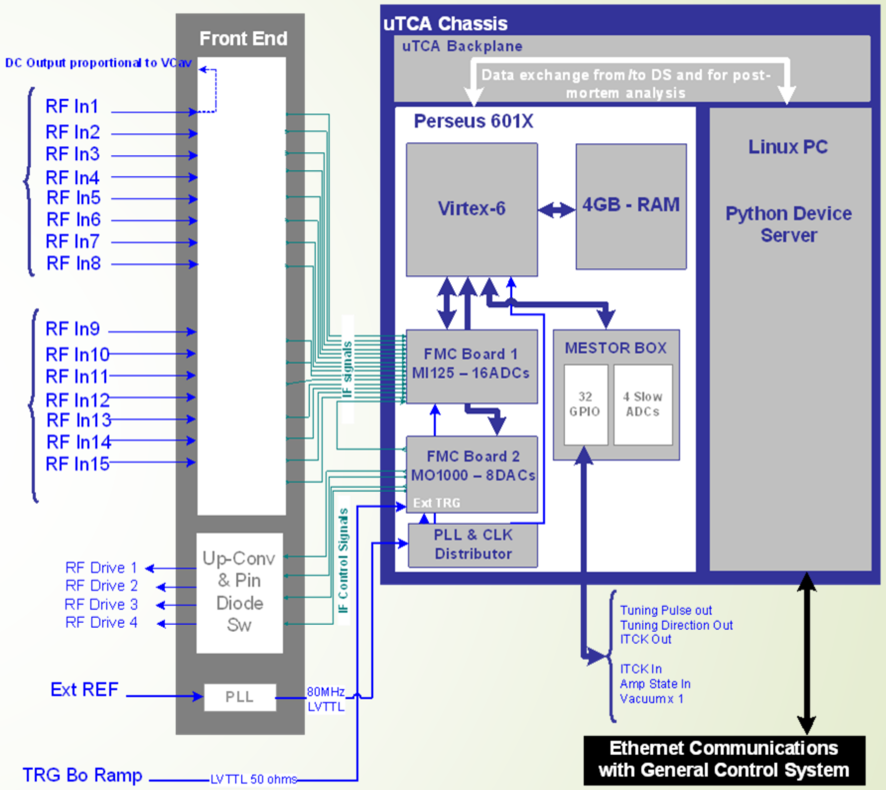




Different from the LLRF probe due to relative amplitude of RF and beam signal.

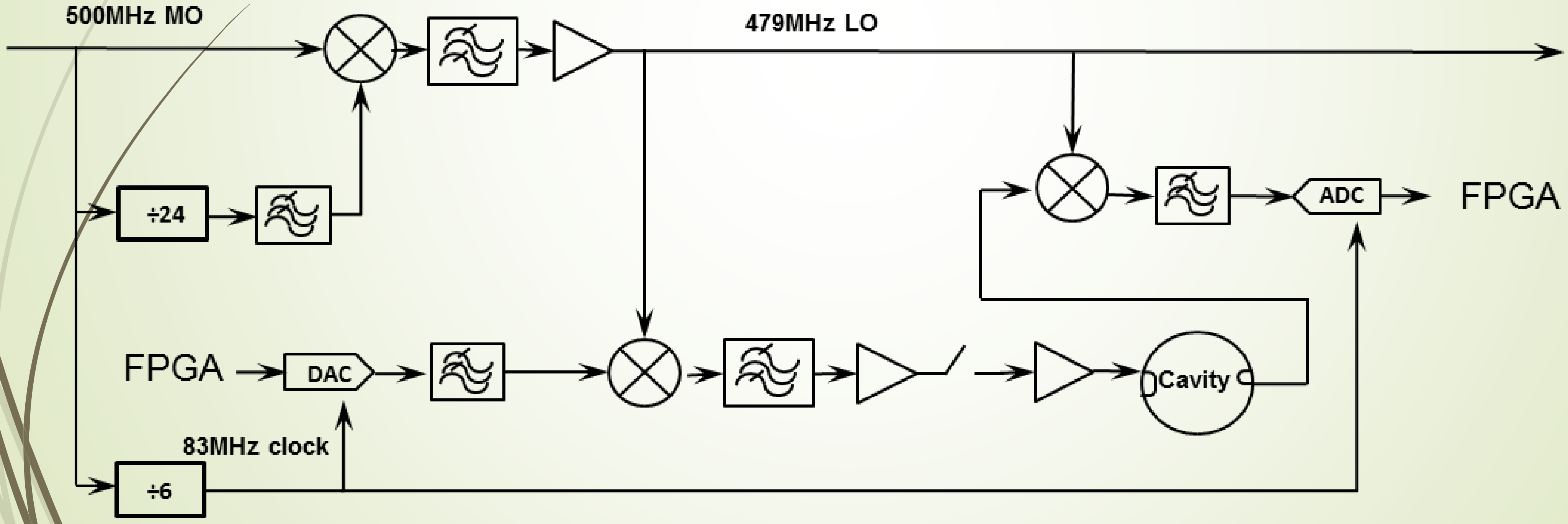
Collaboration with ALBA on Digital LLRF

- New NC cavities will require new LLRF
  - Collaboration with Angela Salom at ALBA
  - Enormous "thank you" to Angela and all at ALBA for providing the DLLRF design and code
- Designed to be a common platform for the control all RF cavities at Diamond
  - Normal conducting cavities
  - Superconducting cavities
  - Booster cavity
- Use one DLLRF unit per cavity in the first instance

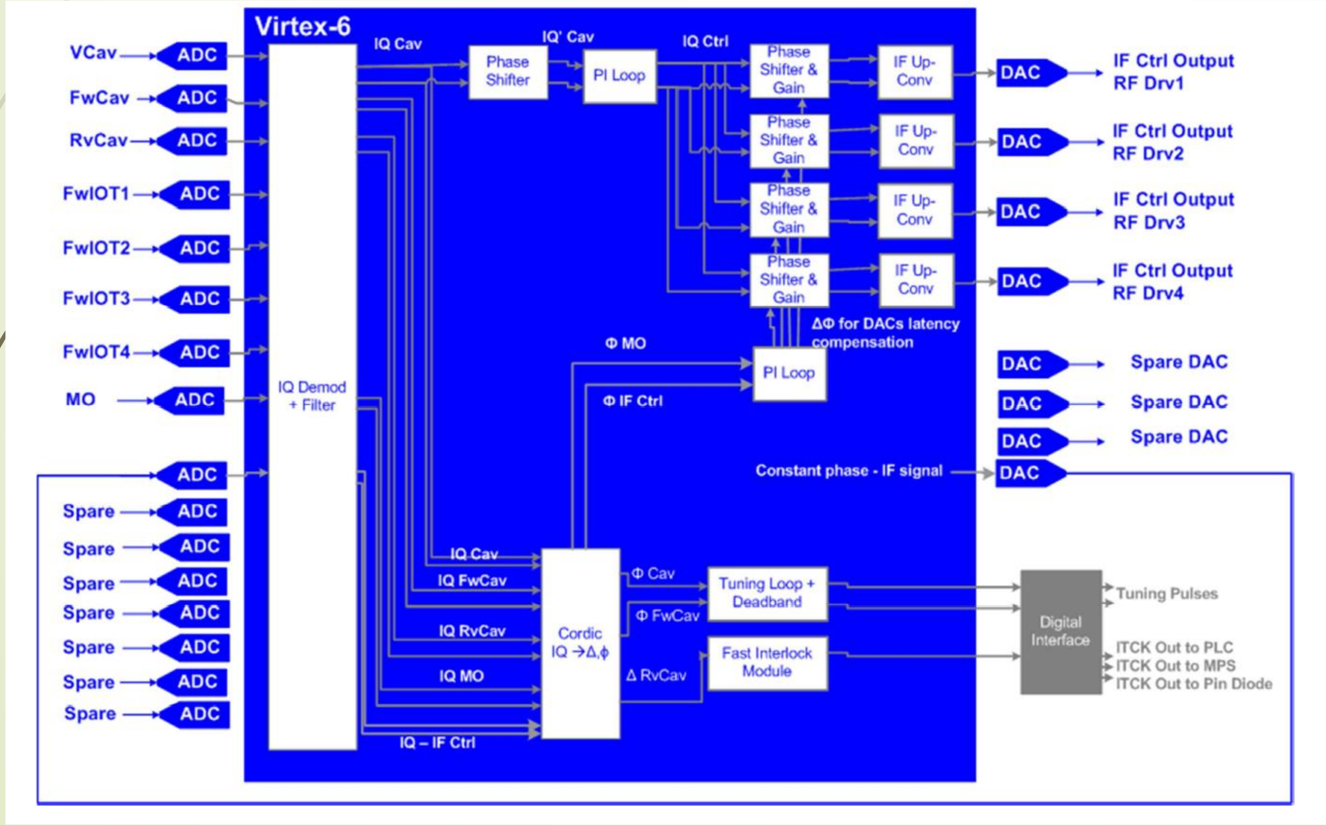


Hardware Configuration

- *Vadatech MTCA*
- *CPU AMC*
- *Nutaq Perseus 601X with Virtex6 FPGA*
- *MO125 16-channel 14-bit 125MSPS ADC FMC*
- *MO1000 8-channel 16-bit DAC FMC*
- *RF frontends: up-converter and down-converter*
- *Digital patch panel*



- IQ or polar PI loops of the cavity field to control amplitude and phase.
- Cavity tuning.
- Fast interlocks handling.
- Automatic start-up of the system.
- Automatic conditioning of the cavity
- Monitoring of RF signals.
- Fast data logging of RF signals for post-mortem analysis.



ADC Test

The raw data from ADCs were retrieved using the fast data logger. Performance was consistent with the specification of the ADC. A 70 dB SNR was achieved.

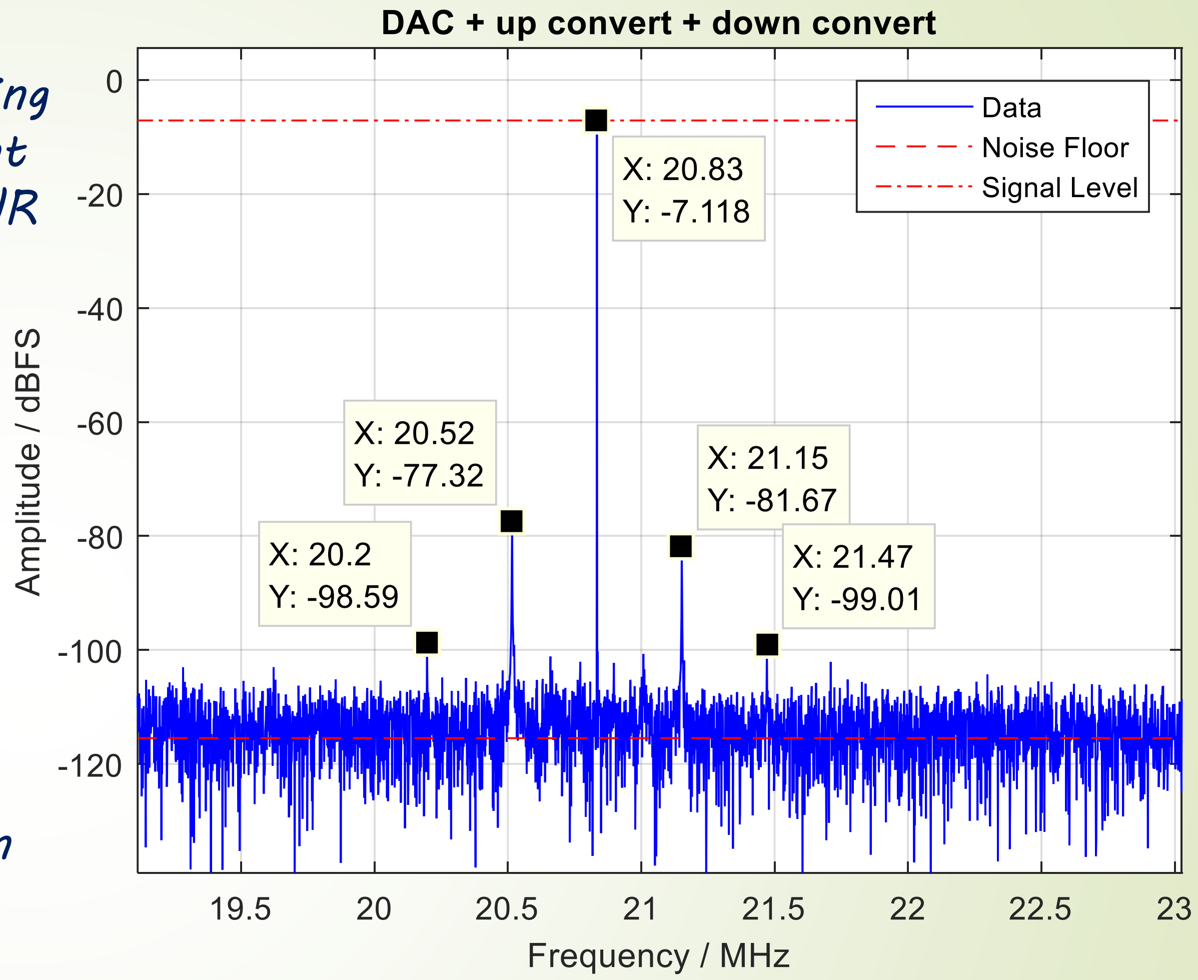
ADC test results

- Amplitude jitter 0.055% RMS
- Phase jitter 0.035° RMS

High Power Test

The new DLLRF was first installed in the booster RF system.

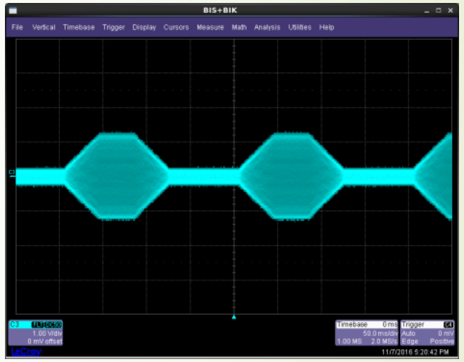
Group delay of the DLLRF was 2.2 μs. Rectangular and polar loops have similar band-width values when using similar proportional gain and integral gain values. 30 kHz bandwidth can be achieved setting high gain values.



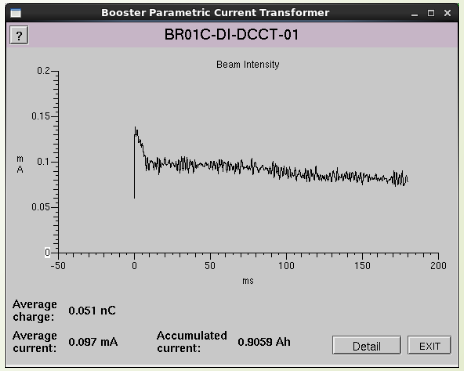
DLLRF tests on the Diamond booster

Diamond booster is in separate tunnel from storage ring, allowing beam tests to be carried out in a machine shutdown

- *DLLRF operation has been demonstrated*
  - *Interfaces allow rapid switch between analogue and digital systems*
  - *Loops have been closed and RF can be maintained*
  - *Beam has been accelerated from 100MeV to 3GeV using DLLRF*



Field

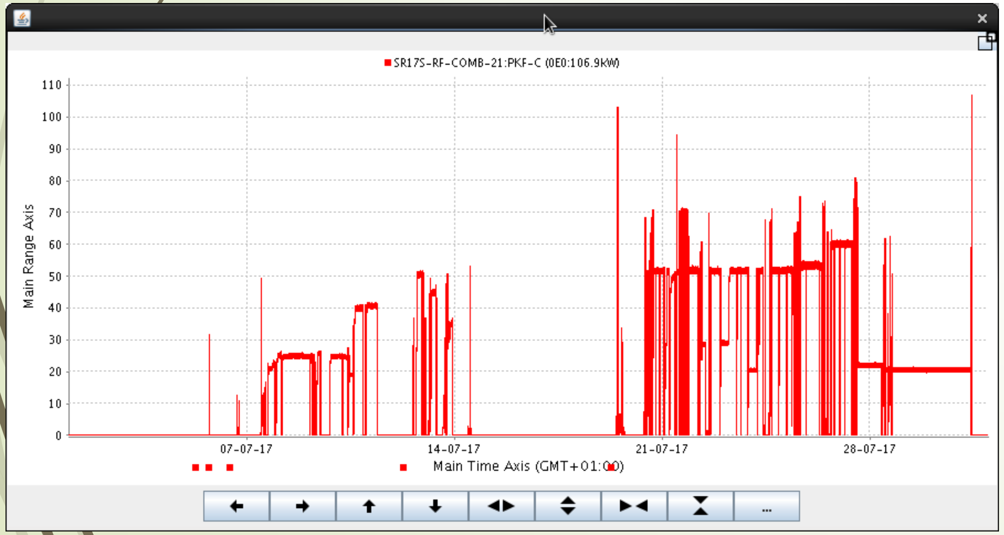


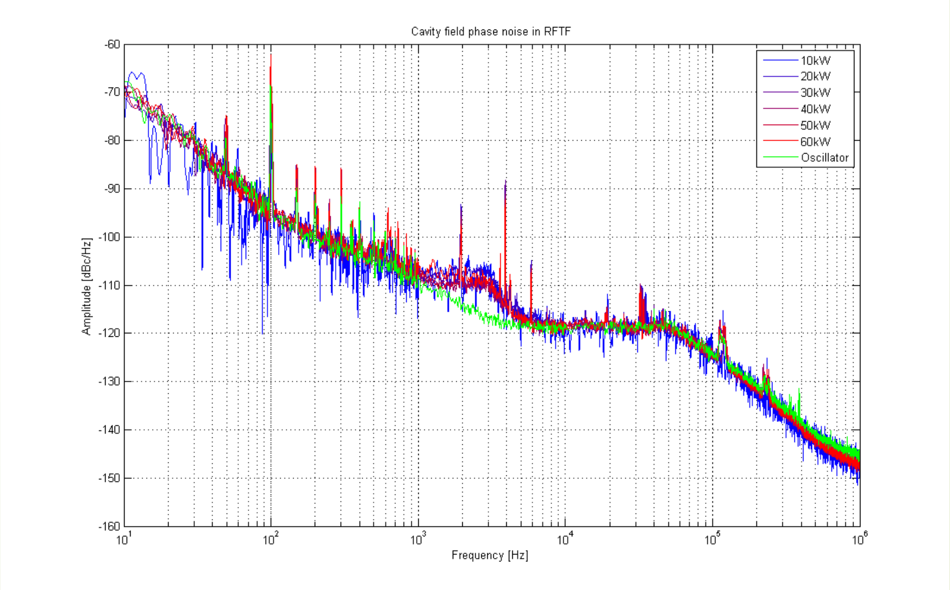
Current

Cavity conditioning in RFTF and deployment in storage ring

Two HOM damped cavities of the BESSY design have been tested in RFTF and installed in the Diamond storage ring. They are controlled by the new DLLRF and have been conditioned to high power using this system. Two DLLRF have been installed for the two NC cavities and testd with beam.

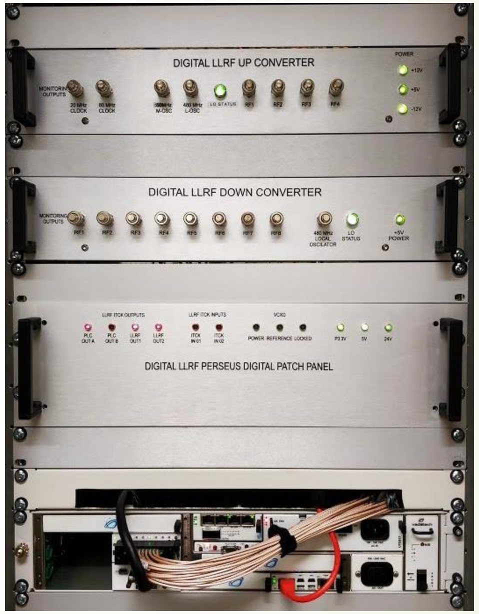
The two cavity was conditioned up to 60kW CW in 2017 and was installed in the storage ring afterwards.
Plots below show the increase in forward power during conditioning and phase noise measured at the pickup at different power levels.





- Total six systems have been built
- Two LLRF systems installed in storage ring for 2 NC cavities
- One LLRF system installed in booster
- One LLRF system installed in RFTF

straight 16



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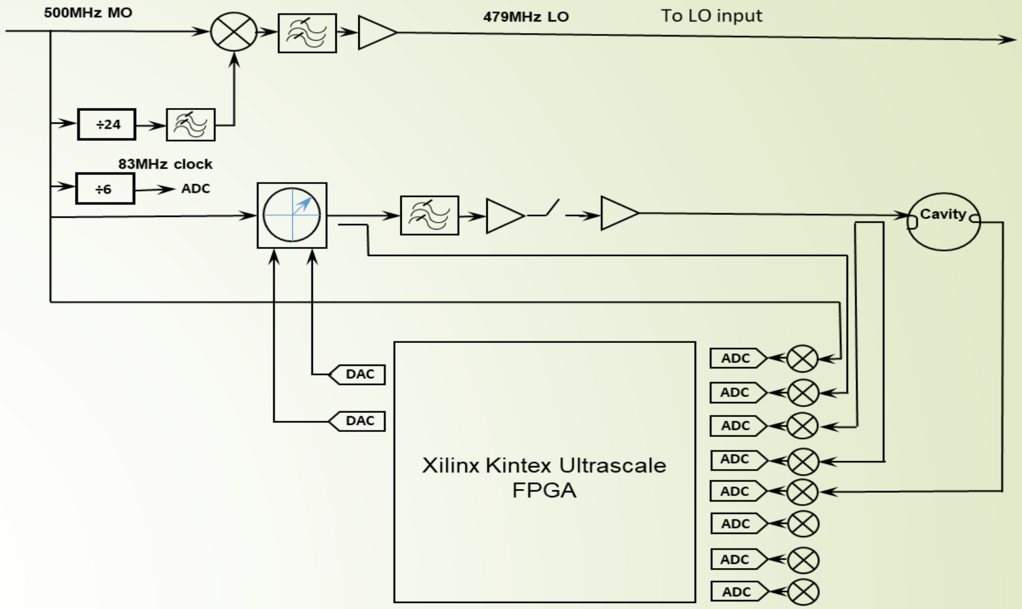
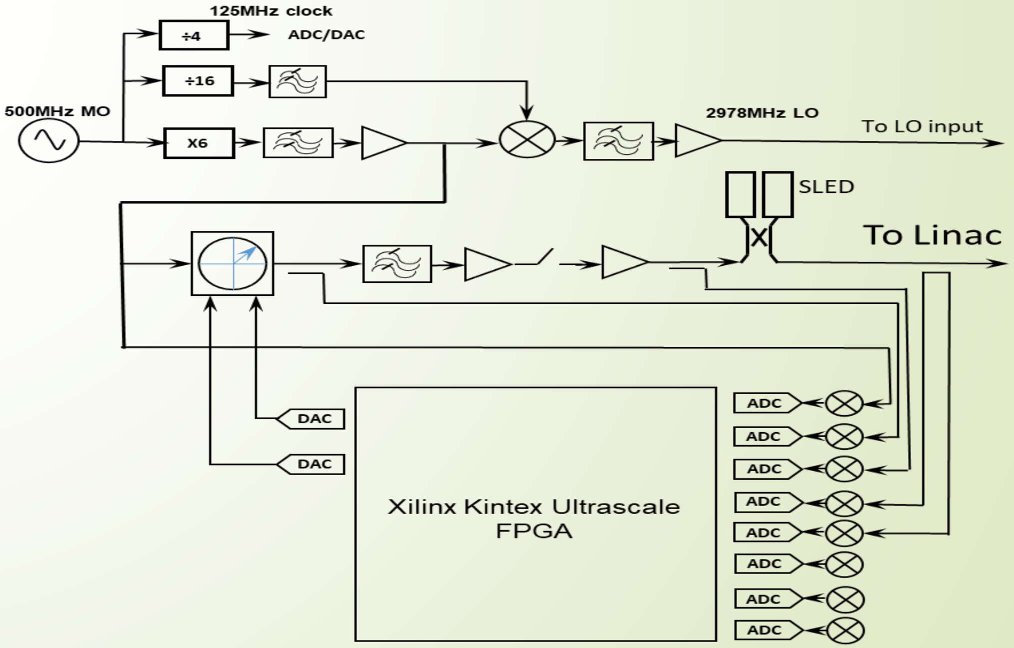
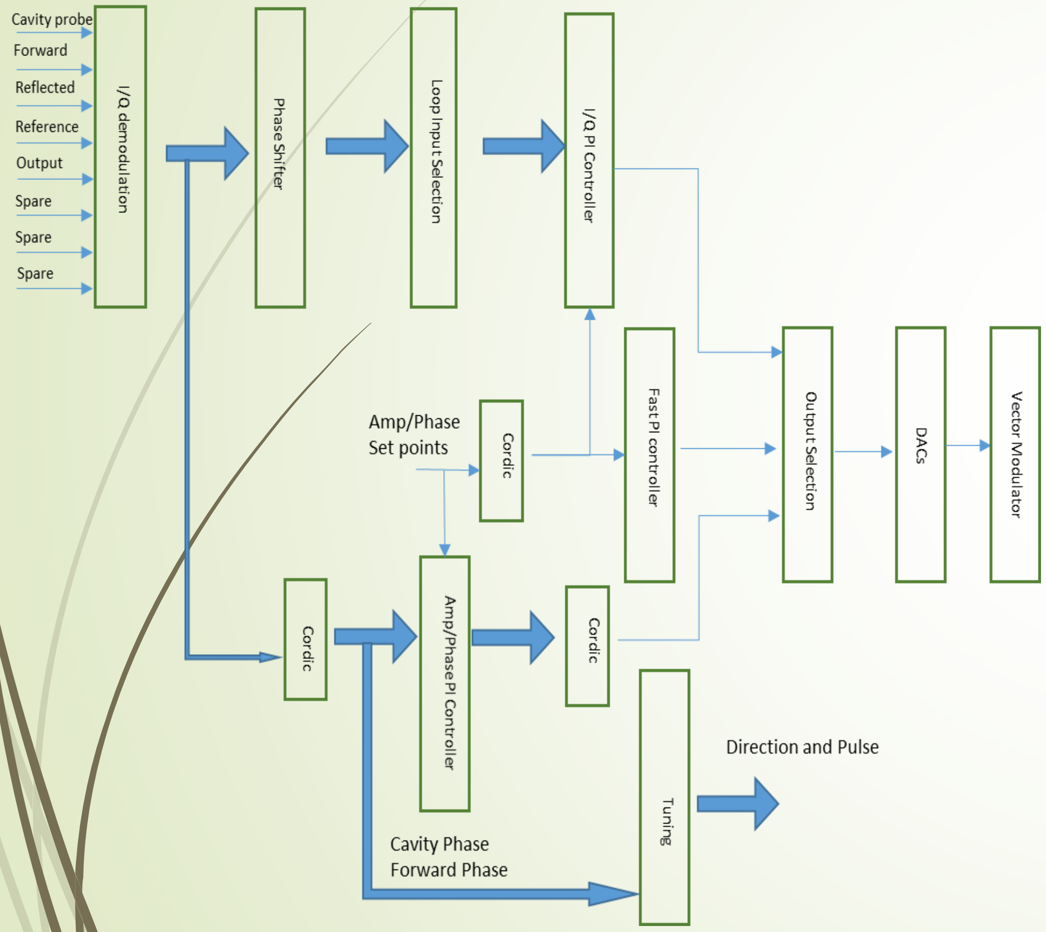
Next DLLRF for Diamond

- One 2U MTCA.4 chassis and MCH
- One Concurrent AMC computer board
- One Struck SIS8300-KU card
- One Struck DWC8VM1 RTM
- Clock/local oscillator (LO)/reference generation RF circuits.
- DI/DO interface

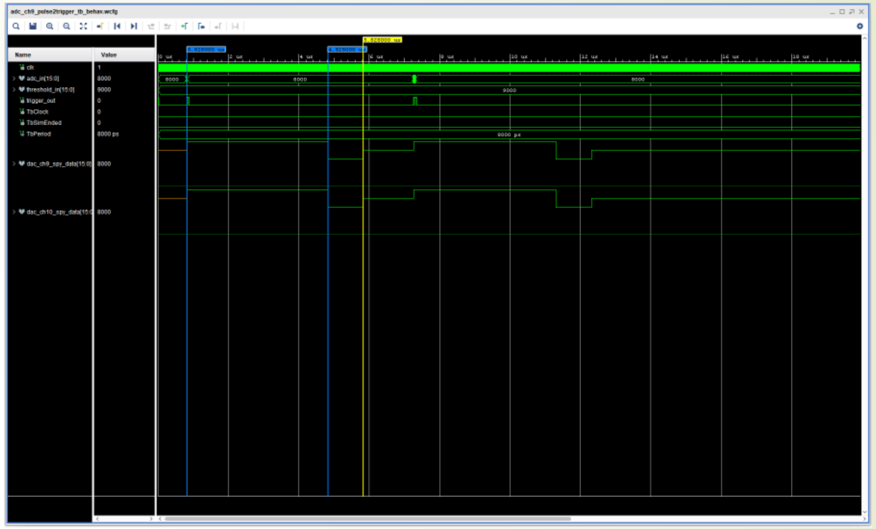




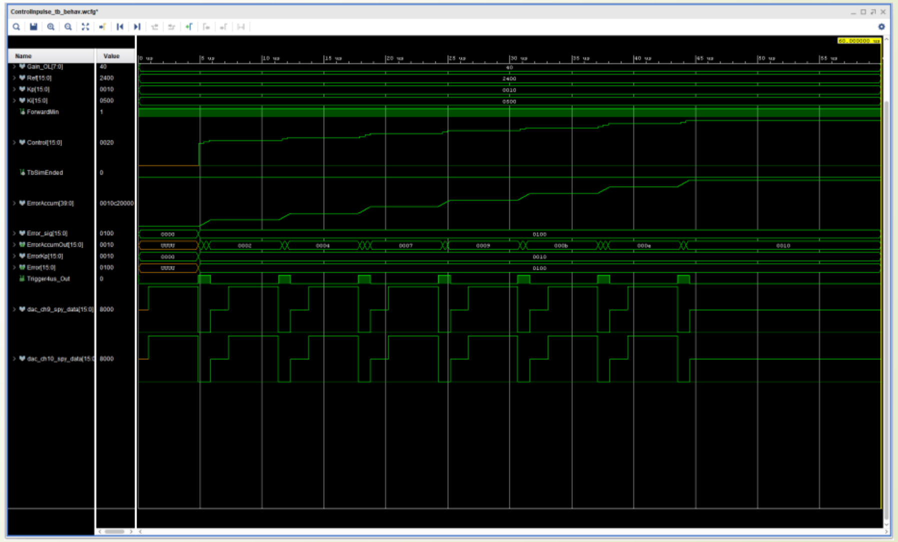
Firmware Development



5 microseconds pulse, with phase flip



Feedback Control only work during the pulse

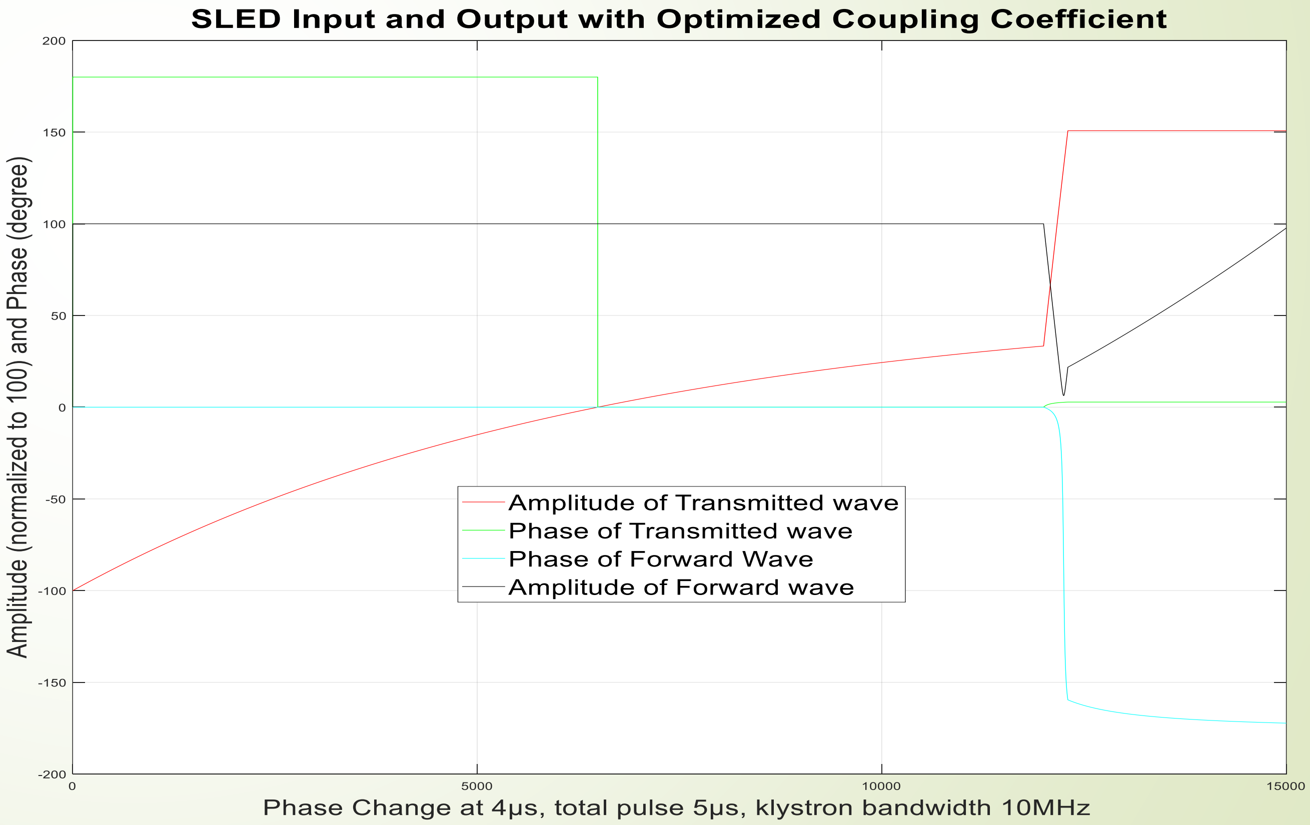


SLED Operation Requirement

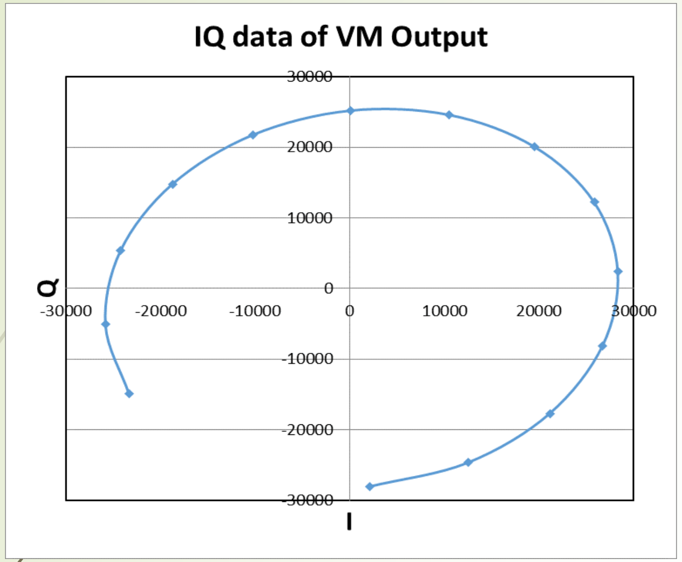
When operating in top-up mode for user beam the linac accelerates a single bunch of electrons, which is compatible with the generation of a peaked power pulse in the simplest mode of SLED operation. To fill the ring, from empty, however, the linac must accelerate a train of up to 120 bunches. A standard phase switch mode operation results in around 7% energy spread and so a flat-top pulse is required. I and Q components of SLED input pulse should follow the equations below.

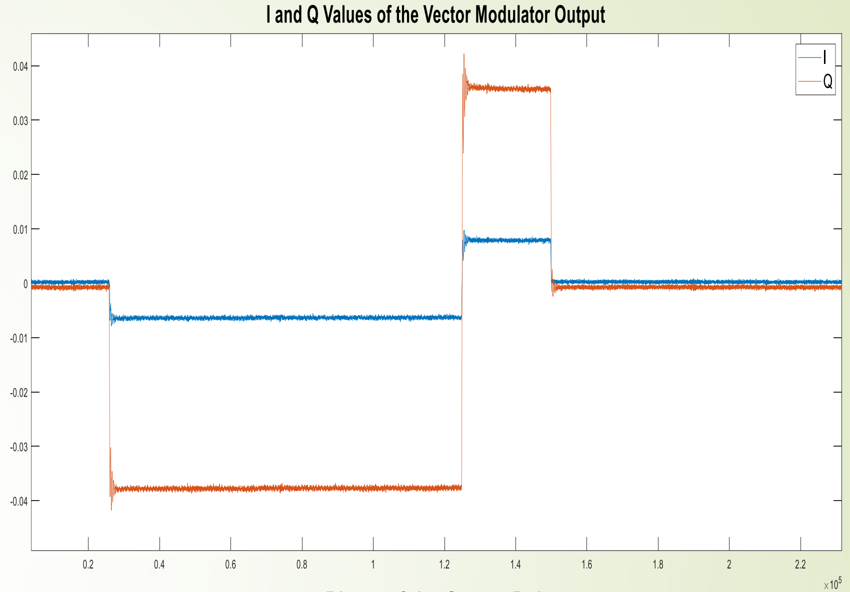
$$F_x = \frac{R_x}{\alpha - 1} + \alpha\left(1 - e^{-\frac{t1}{Tc}} - \frac{R_x}{\alpha - 1}\right) e^{-\frac{(\alpha-1)(t-t1)}{Tc}}$$

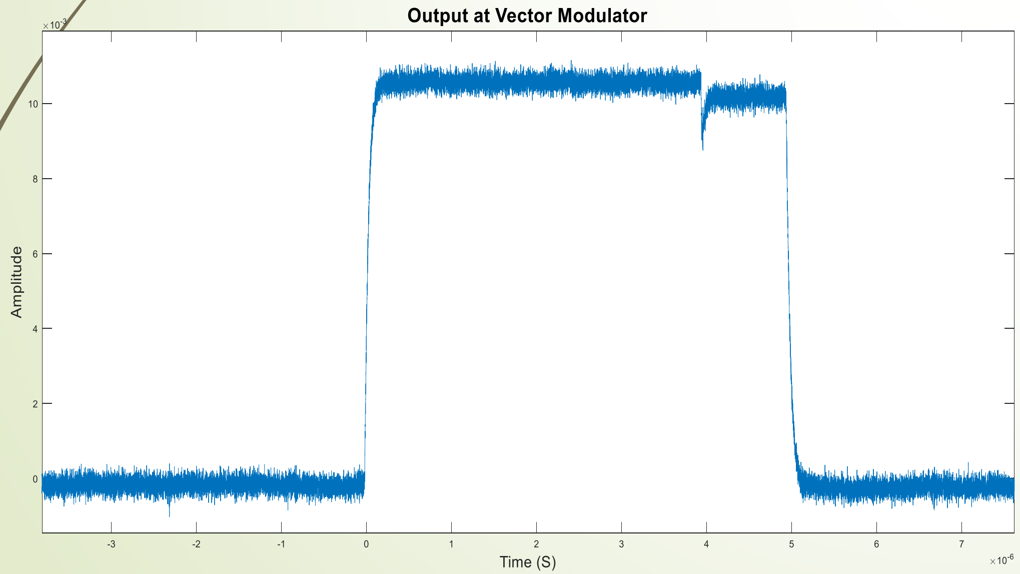
$$F_y = \frac{R_y}{\alpha - 1} - \frac{\alpha R_y}{\alpha - 1} e^{-\frac{(\alpha-1)(t-t1)}{Tc}}$$

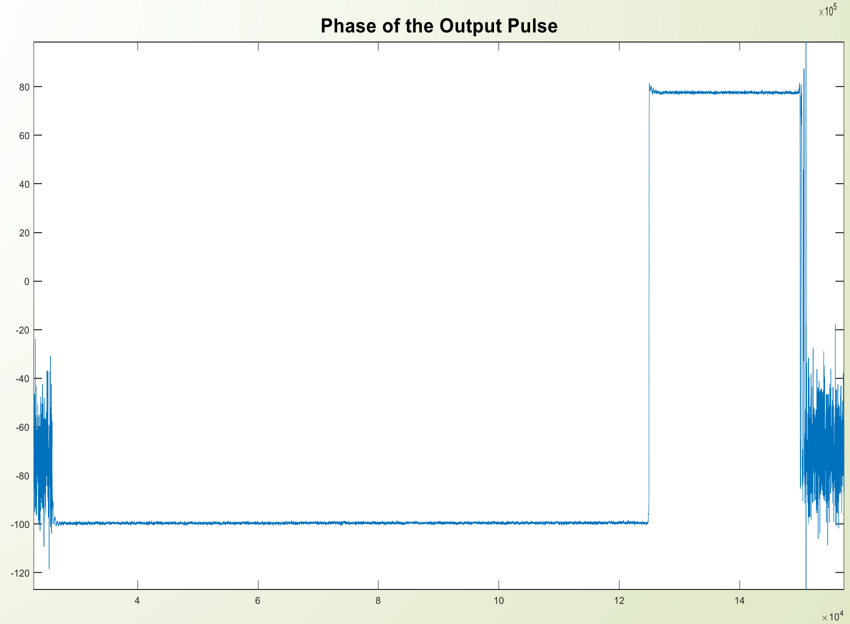


Some Initial Test Results in the Lab





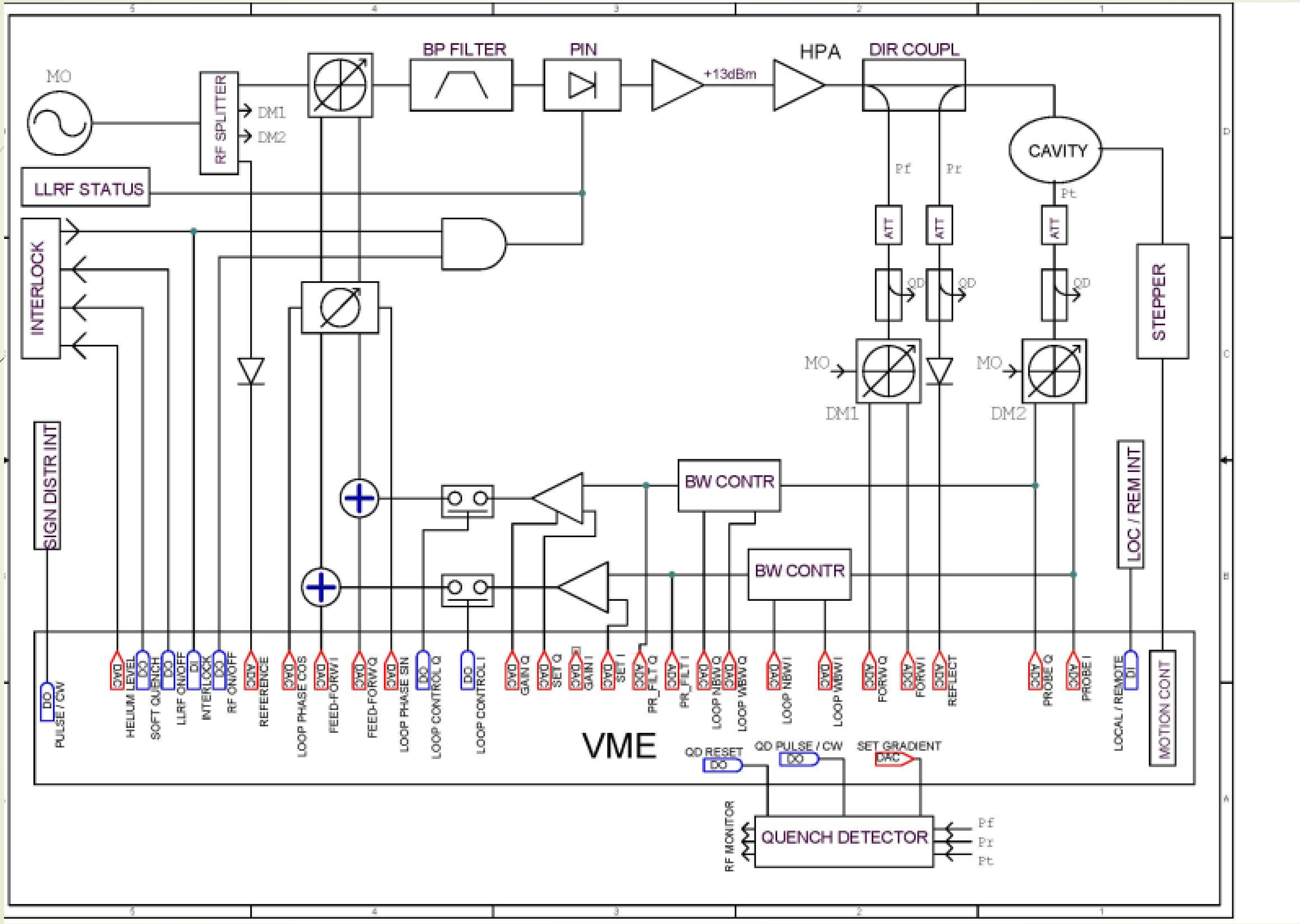




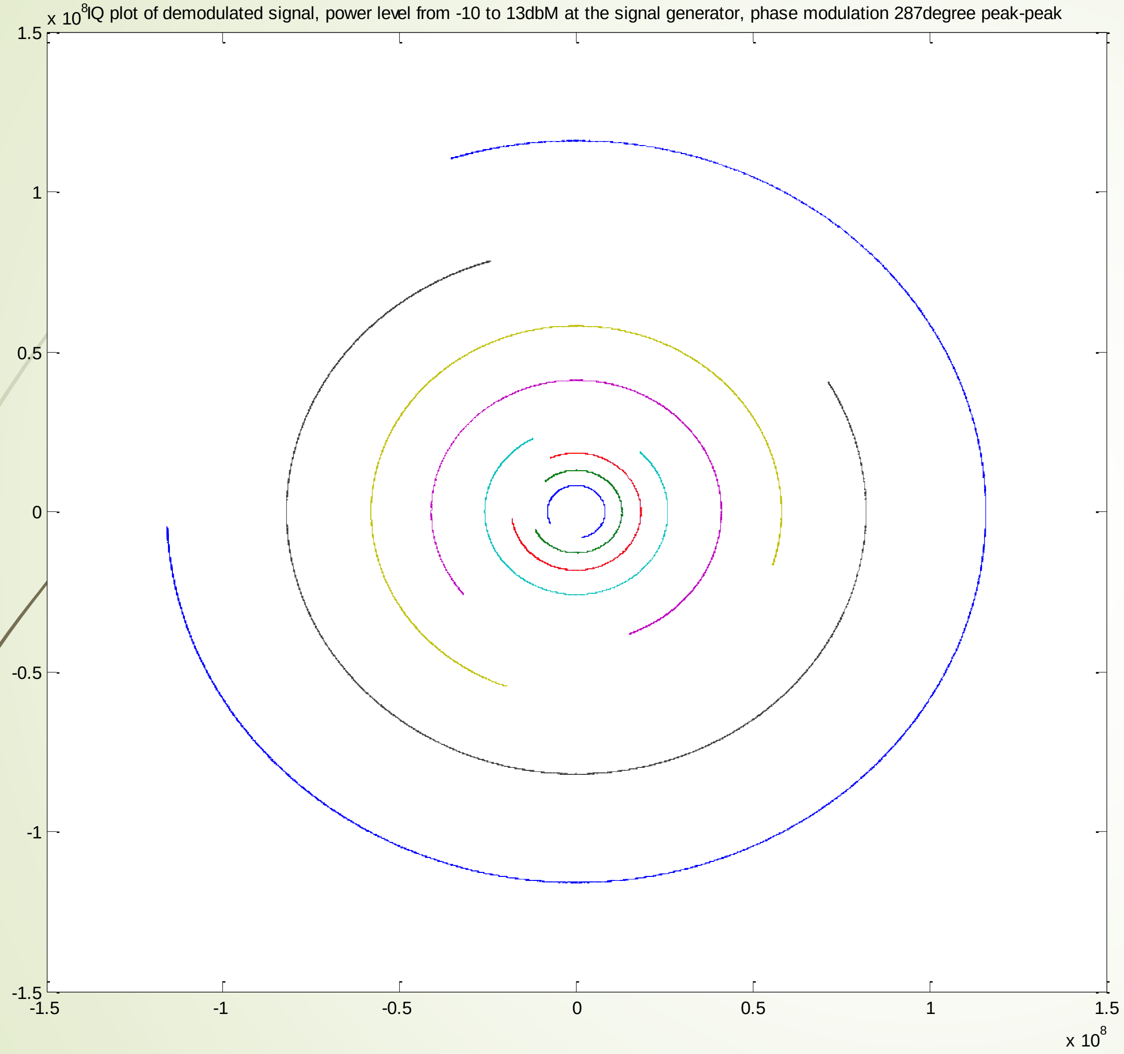
Thank You!

Backup slides

Storage Ring Analogue LLRF



IQ Plot of Demodulated Signal from -10 to 13dBm with 287degree Phase Modulation



Phase measurement at different power levels.

Minimal distortion over dynamic range

Advantages of this method:

- *No imbalance between I and Q channels often observed using IQ demodulators*
- *No DC offset errors*

Test in the Lab, direct sampling @2GSPS