# Soleil LLRF Activities

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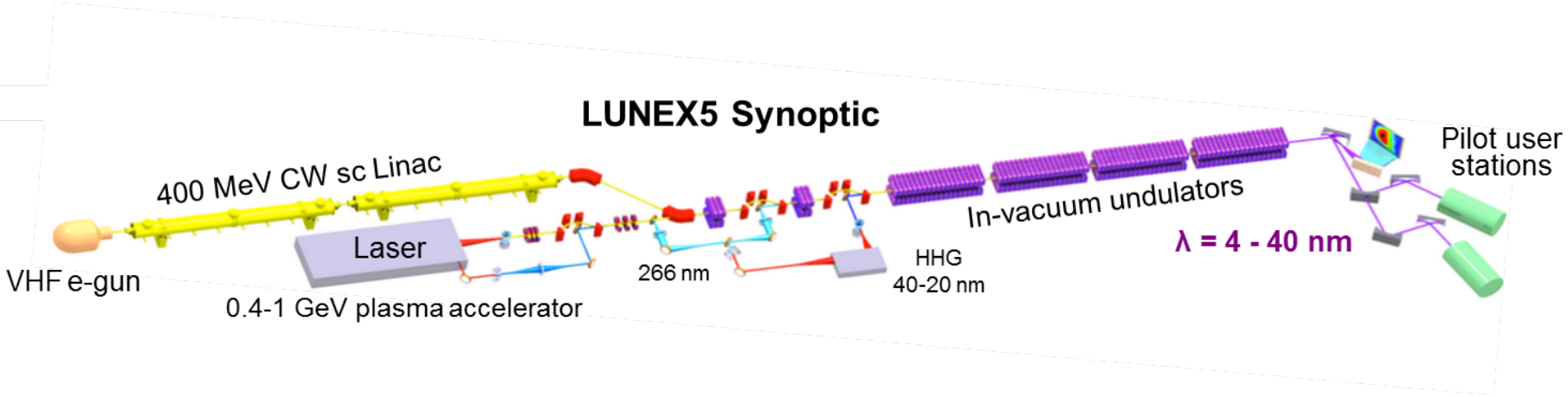
# Content

- LUCRECE/LUNEX5 LLRF progress
- Aim : to have a common platform
- Digital µTCA.4 platform for new projects

# Contribution to LUCRECE/LUNEX5



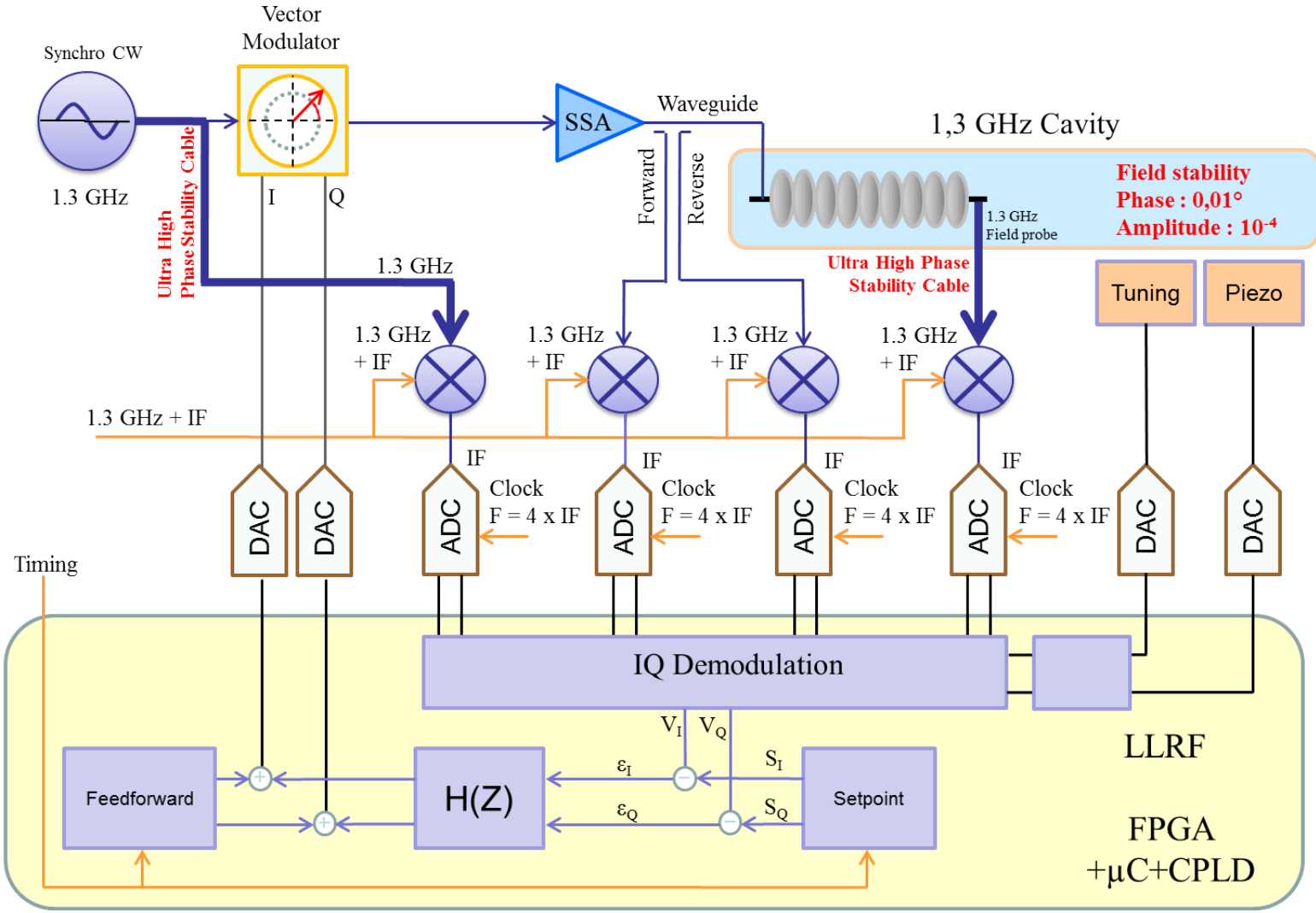

**Phase 1 : based on a 400 MeV CW sc Linac → explore advanced FEL techniques and applications**
**Phase 2 : laser wakefield (or plasma) accelerator will be assessed in view of FEL applications**

- **LUCRECE : program of R&D about RF technology for CW Linacs, with the aim to LUNEX5**

**It is coordinated by SOLEIL, involves the CEA and CNRS labs as well as industrial partners, Thales, Alsyom and SigmaPhi Electronics (SPE) ; partly financed by the Region Ile-de-France.**

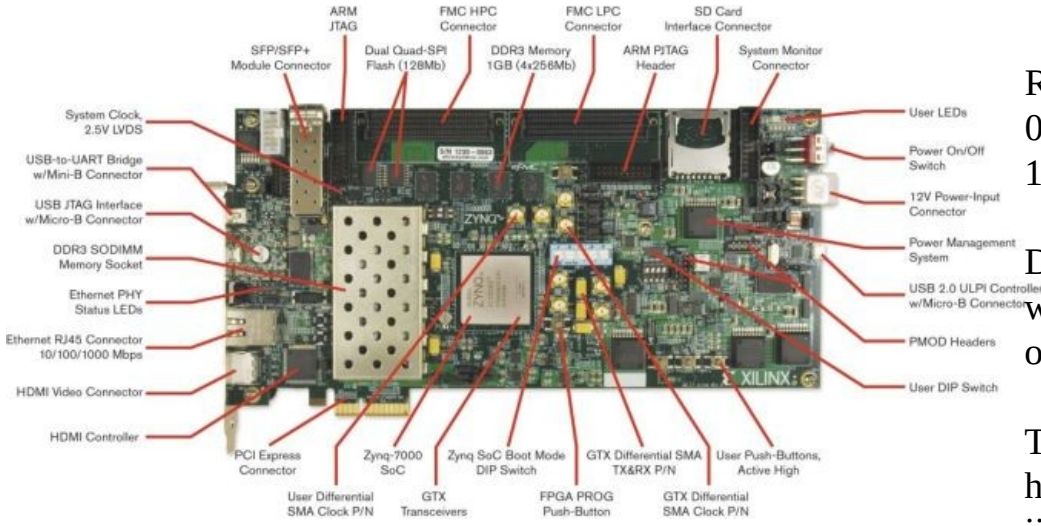
→M.Diop's talk

# LUCRECE LLRF basic design



# LUCRECE LLRF: choice of technology

FPGA Xilinx SoC ZC706 (Zynq-7000) board




RF cavity field stability requirements are :
0.01 ° in phase and $10^{-4}$ in amplitude
1 LLRF + 1 SSA per cavity.

Digiatl LLRF based on IQ (or non-IQ) demodulation will give all the flexibility to implement different operating modes (CW or pulsed).

The main characteristic of ADCs and DACs are high bit resolution, good signal-to-noise ratio , low jitter and low latency in order to meet the required stability performance.

4 channel ADC FMC board (TECHWAY)

## Complete LLRF design in collaboration with LAL (Orsay)

- R&D, component choice
- Component performance test
- Production of the complete system
- Test with the cavity

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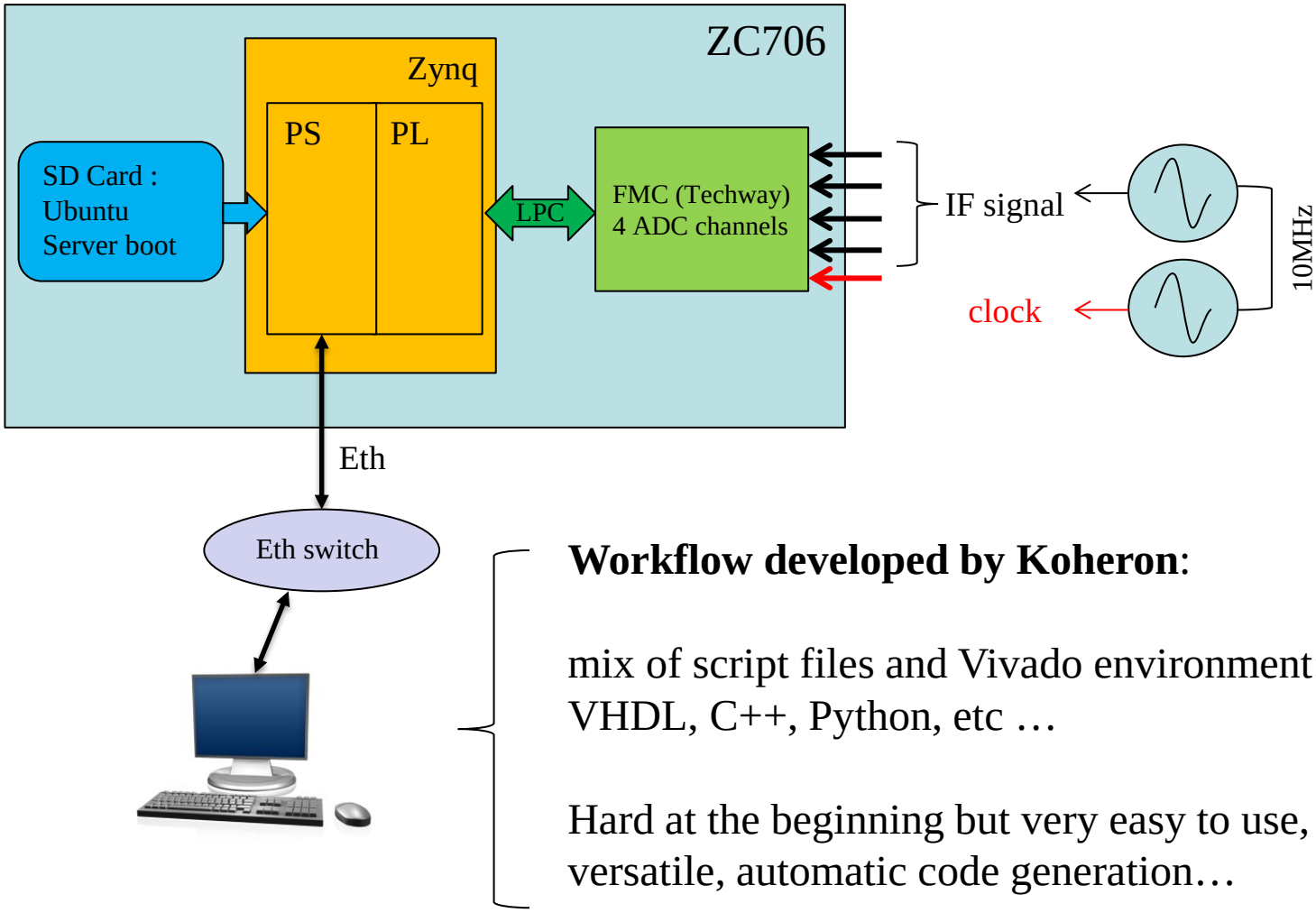
# LUCRECE LLRF: choice of technology

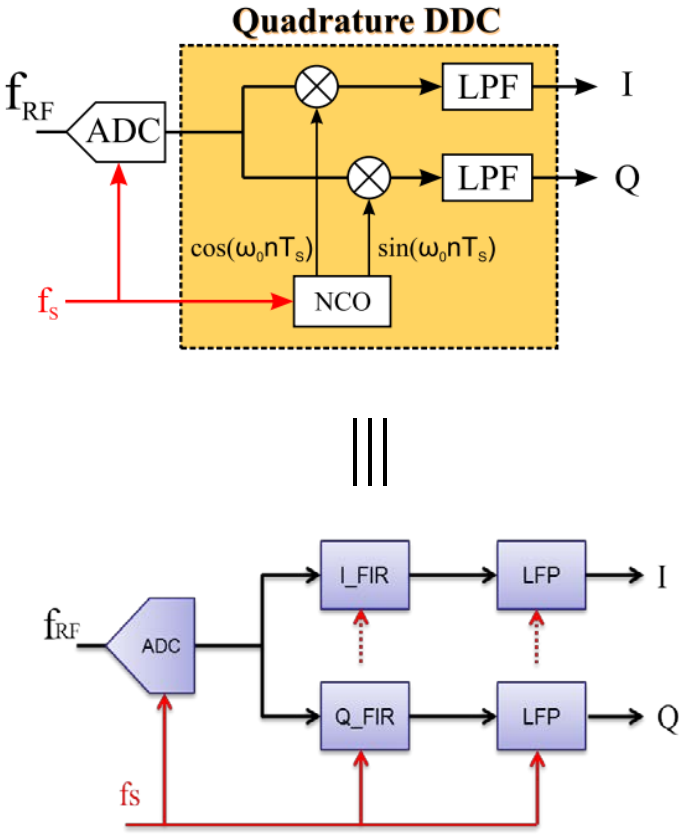



**Workflow developed by Koheron**:

mix of script files and Vivado environment: VHDL, C++, Python, etc …

Hard at the beginning but very easy to use, versatile, automatic code generation…

# Digital non-IQ demodulation method




$M \cdot f_{RF} = N \cdot fs$ $\quad\quad$ $\Delta\varphi = 2\Pi \cdot N/M$

$$I = 2/M \sum_{i=0}^{M} yi \cdot \cos(i \cdot \Delta\varphi)$$

$$Q = 2/M \sum_{i=0}^{M} yi \cdot \sin(i \cdot \Delta\varphi)$$

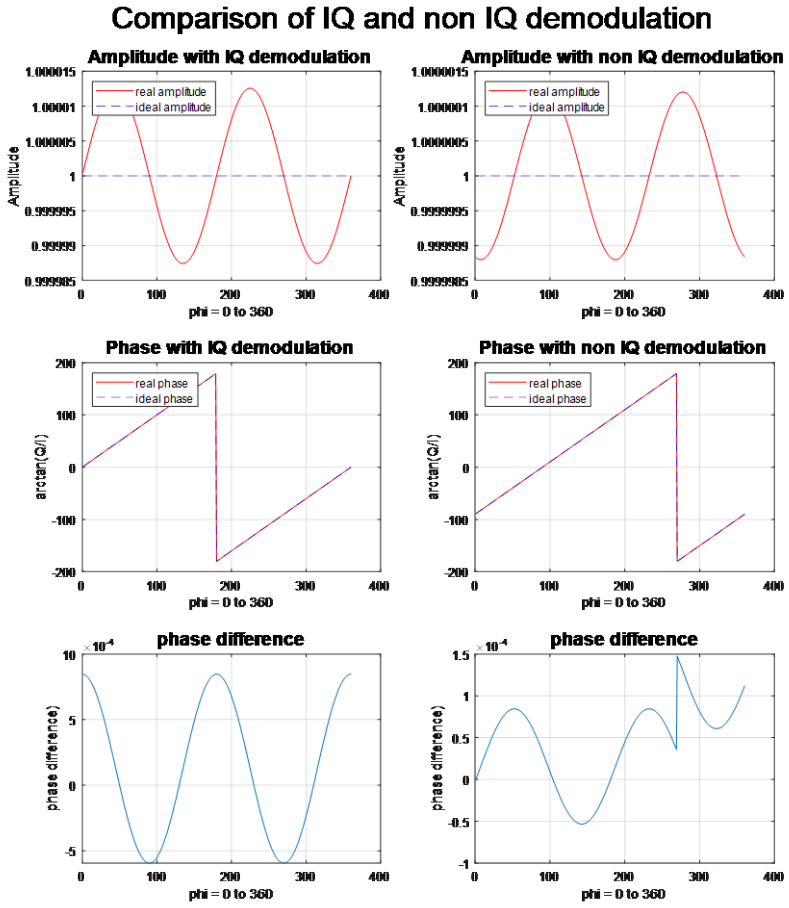
$Coef\_FIR\_I(i) = \cos(i \cdot \Delta\varphi)$

$Coef\_FIR\_Q(i) = \sin(i \cdot \Delta\varphi)$

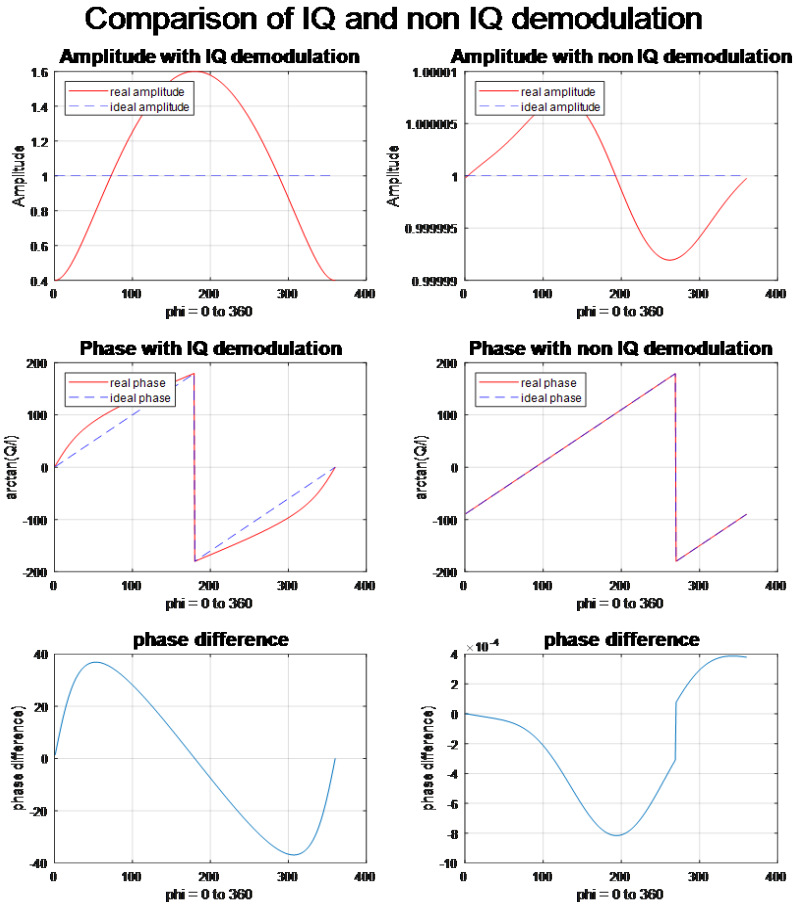
By down-sampling a RF signal, we can calculate precisely I and Q.
But we need few RF period instead of one with a classical IQ demodulation.

# Digital non-IQ demodulation method

Matlab simulation done by our new RF engineer trainee (B. Chelaoui):
Comparison IQ vs non-IQ with some harmonics introduction on the IF signal



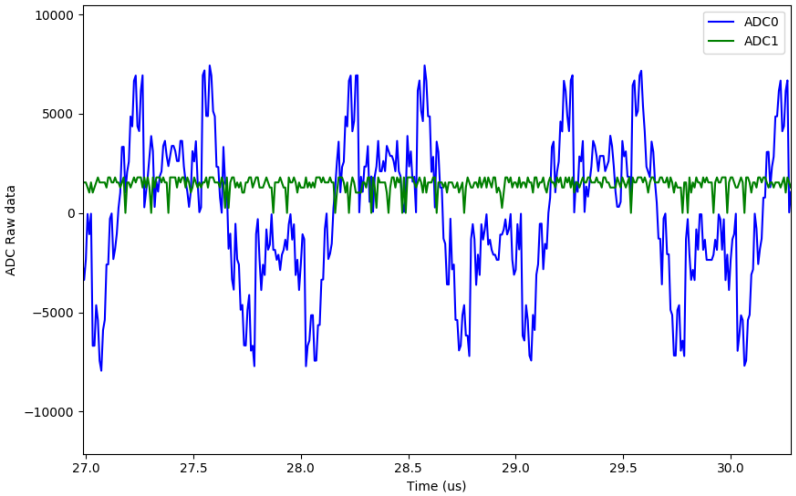

With jitter and without harmonics



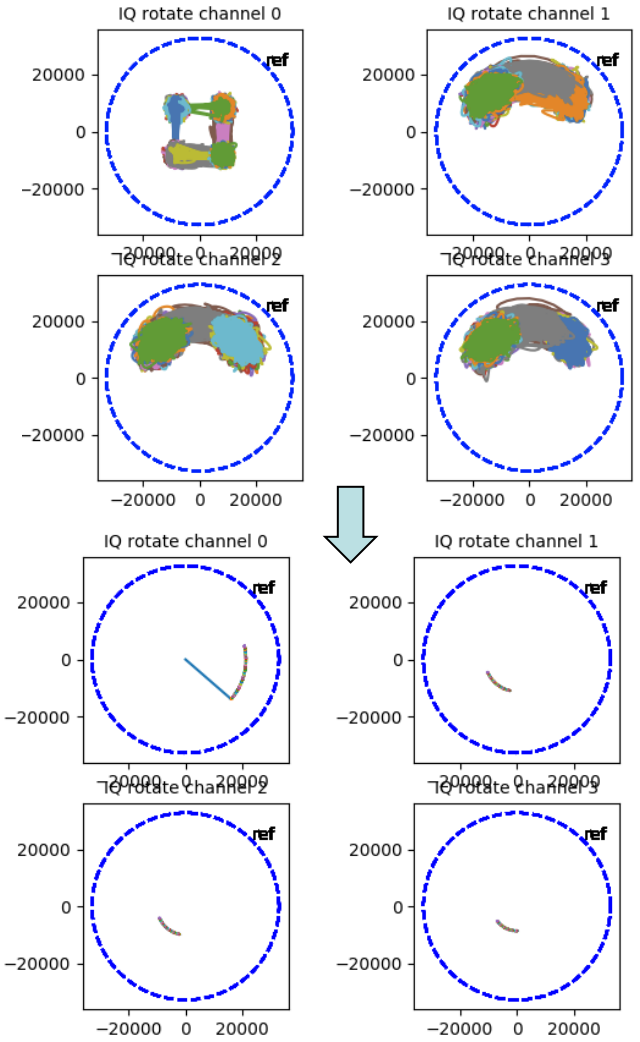

With jitter and harmonics

# Preliminary tests: pleasure of debug

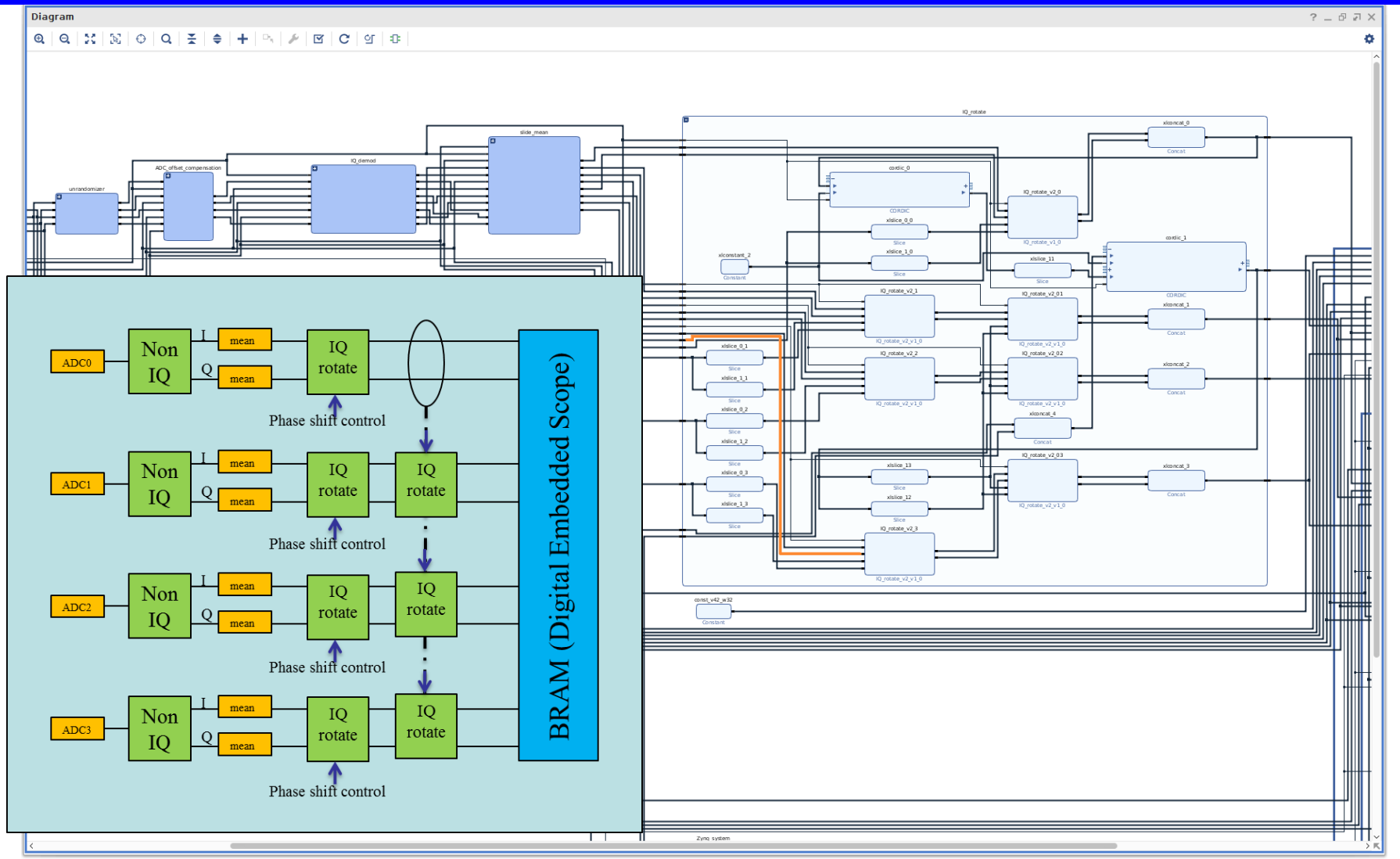
## 4 ADC channels acquisition




## 4 IQ rotate channels




# LLRF: Zynq building blocks




$$\frac{F_{RF}}{F_s} = \frac{N}{M} = \frac{4}{9}$$

With this ratio and 64 values of sliding mean, real measurements give 0.02° rms. We have to improve it and test other ratios.

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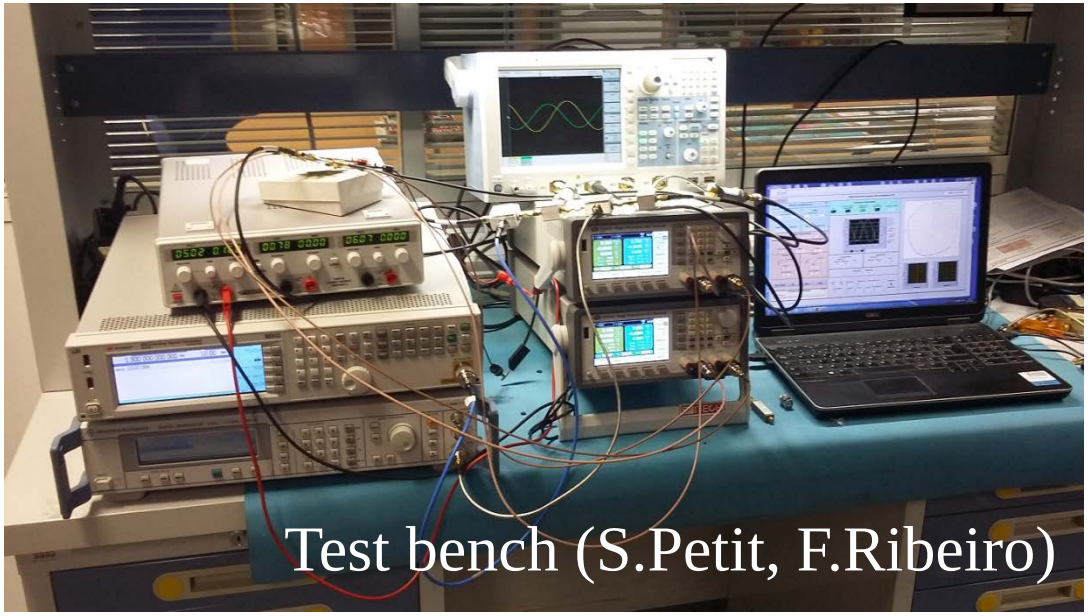
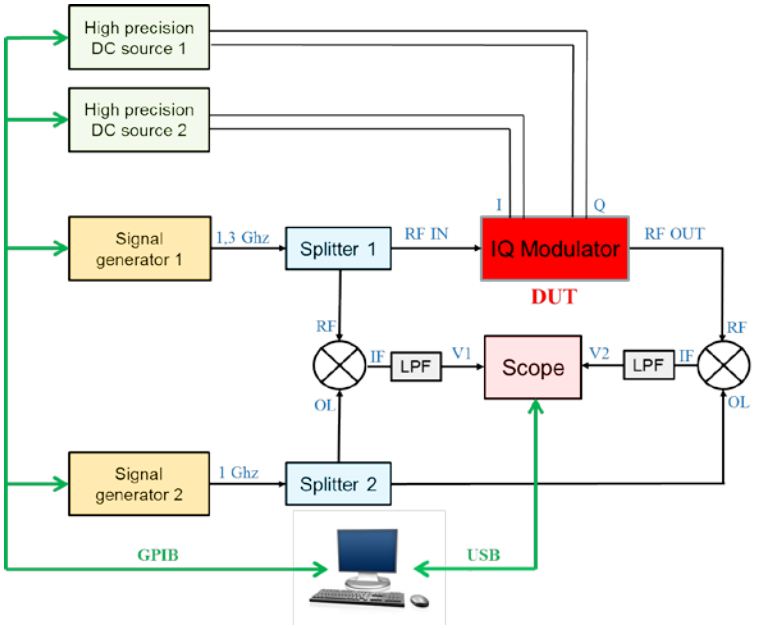
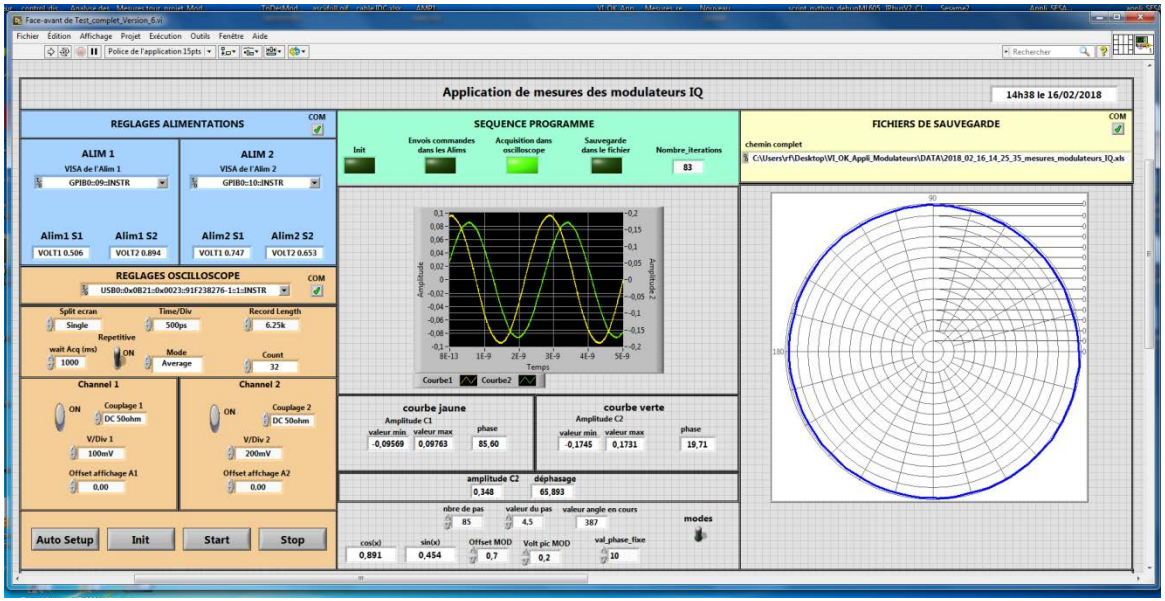
# RF Analog component characterization




We have tested:
**LTC5598**
AD8345
TRF370333
…
We have selected **LTC5598** for its good linearity.

# Native-R2 µTCA platform

The NATIVE-R2 is a 2U MTCA.4 chassis particularly suited to telecommunications, industrial and particle physics research applications.

Supporting a single MCH and one power unit, the NATIVE-R2 can accommodate six horizontally-mounted AMC modules (five mid-size and one full-size), up to five MicroRTMs (uRTM), and one JTAG switch module (JSM).

This enables you to build a compact, multi-purpose computing system for a variety of applications by integrating cost-effective AMCs. The compact design and support for PCIe Gen3 x8 makes the NATIVE-R2 ideal for applications with high connectivity requirements, such as high energy physics and telecom edge, access and aggregation equipment.

**2U MTCA.4 chassis - up to 6 AMCs, support for PCIe Gen3 x8**

<table>
<tr><td>AMC 1</td><td>AMC 5</td><td rowspan="4">CU</td></tr>
<tr><td>AMC 2</td><td rowspan="2">MCH</td></tr>
<tr><td>AMC 3</td></tr>
<tr><td>AMC 4</td><td>AMC 6</td></tr>
</table>

<table>
<tr><td rowspan="4">CU</td><td>AMC RTM 5</td><td>AMC RTM 1</td></tr>
<tr><td rowspan="2">MCH RTM</td><td>AMC RTM 2</td></tr>
<tr><td>AMC RTM 3</td></tr>
<tr><td rowspan="2">PU</td><td>AMC RTM 4</td></tr>
</table>

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# AMC580 board from Vadatech

**AMC580**

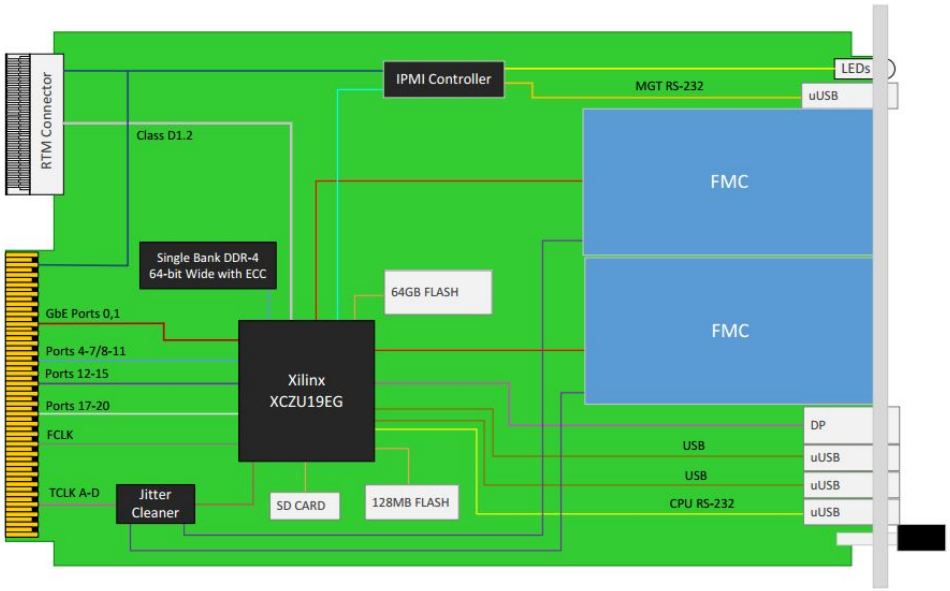
The AMC580 is an AMC FPGA Carrier with dual FMC (VITA-57) interfaces.
The unit has an on-board, re-configurable FPGA which interfaces directly to the AMC FCLKA, TCLKA-D, FMC DP0-9 and all FMC LA/HA/HB pairs.

The FPGA has an interface to a single DDR4 memory channel (64-bit wide with ECC). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The AMC is based on Xilinx UltraScale+ XCZU19EG MPSoC FPGA with dual FMC sites. The RTM (Rear Transition Module) pinout is compatible to the DESY D1.2 specification.

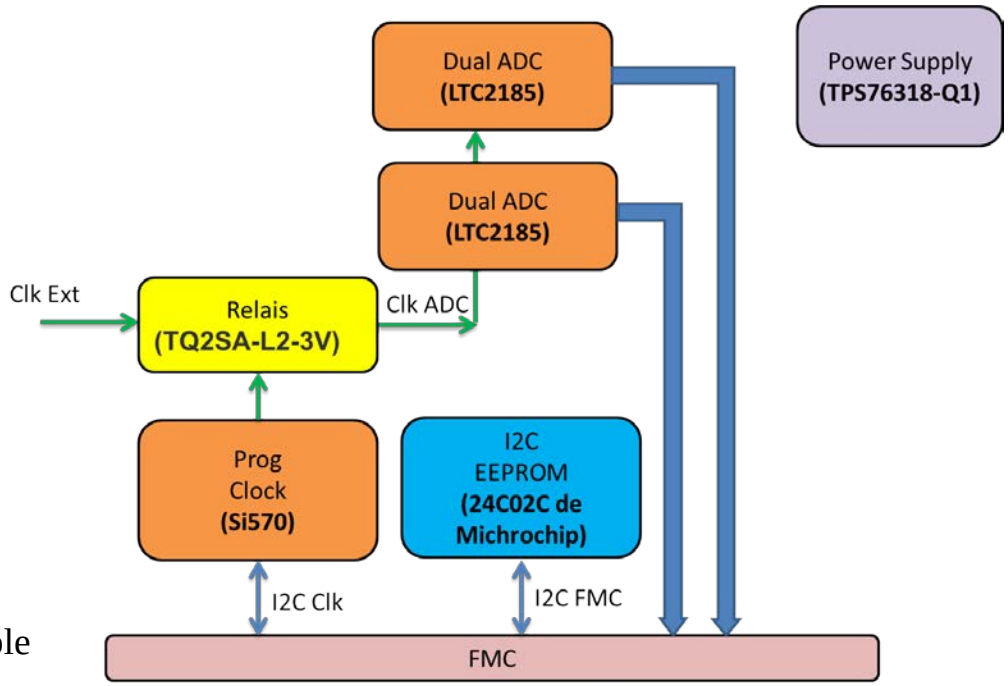
The FPGA has 1968 DSP Slices and 1143k logic cells. The XCZU19EG includes a quad-core ARM processor.
The Module has on board 64 GB of Flash, 128 MB of boot flash and an SD Card as an option.

Block Diagram




# FMC ADC board from TECHWAY

**4 channels ADC FMC board (TECHWAY)**

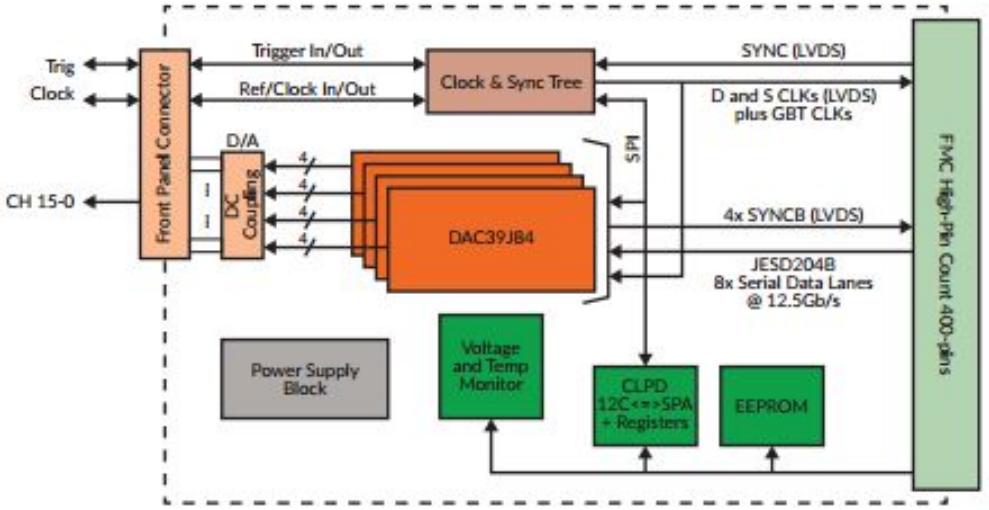



**Four Sampling Channels**

- One common trigger input
- One common sampling clock input
- Internal programmable clock generator available
- Selected sampling clock from external or local

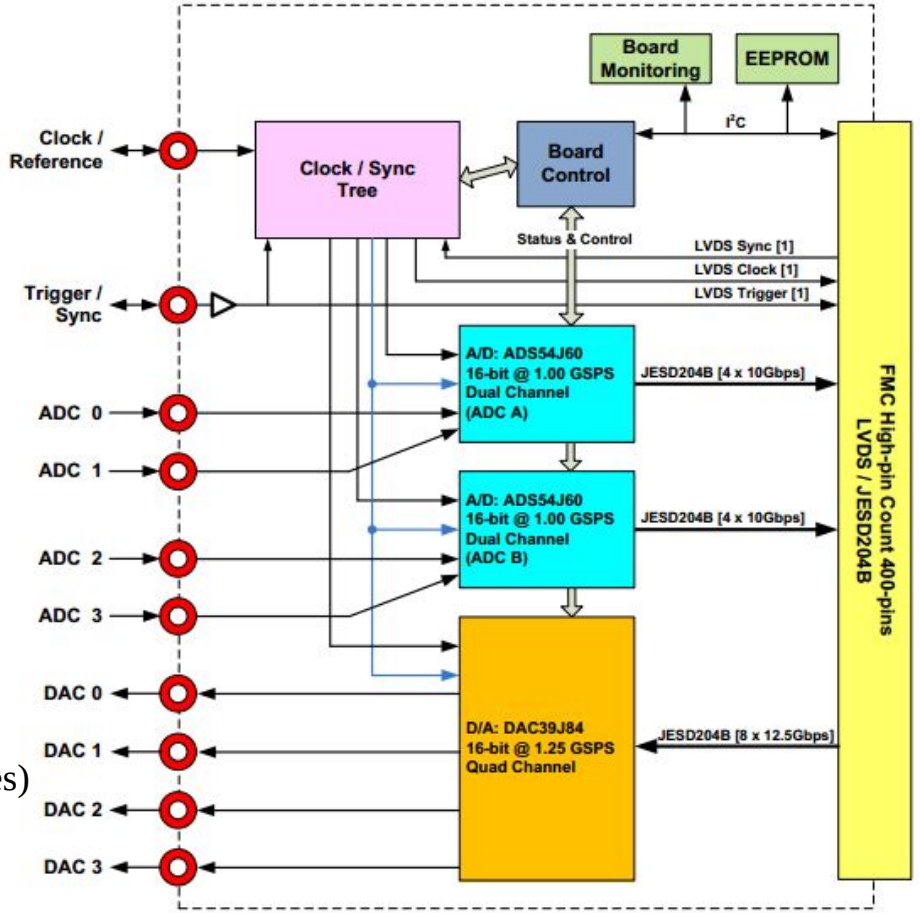
- 16 bits resolution
- Input range: 1Vpp
- Up to 125MHz sampling frequency
- Up to 550MHz analog bandwidth (depend of input analog stage)
- Up to 90dB SFDR
- **Up to 77 dB SNR**

# FMC208 DAC board from 4DSP




4 (CH0-CH7 for FMC204)
**Channel resolution:** 16-bit
**Output voltage range:** 2.0Vpp DC Coupled into 50Ω (+10dBm)
**Output impedance:** 50Ω
**Crosstalk :** -50dBFS typical at 30 MHz, -40dBFS typical at 50MHz, -30dBFS typical at 100MHz
**Analog output bandwidth:** DC Coupled -1.0dB typical at 80MHz, -1.7dB typical at 103MHz, -3.0dB typical at 120MHz
**SFDR:** -50dBFS typical
**Harmonics :** F2 -50dBFS typical, F3 -50dBFS typical, F4 -70dBFS typical, F5 -70dBFS typical
**DAC Input Data width :** JESD204B 4 or 8-pairs
**Sampling Frequency Range:** up to 312.5Msps → This may be further limited by JESD204B channel bandwidth.

# FMC120 ADC/DAC board from 4DSP




ADC Characteristics

- 16-Bit Resolution, Dual-Channel, 1-GSPS ADC
- Noise Floor: –159 dBFS/Hz
- Spectral Performance (fIN = 170 MHz at –1 dBFS):
  - **SNR: 70 dBFS – NSD: –157 dBFS/Hz**
  - SFDR: 86 dBc (Including Interleaving Tones)
  - SFDR: 89 dBc (Except HD2, HD3, and Interleaving Tones)
- Spectral Performance (fIN = 350 MHz at –1 dBFS):
  - **SNR: 67.5 dBFS**
  - NSD: –154.5 dBFS/Hz
  - SFDR: 75 dBc
  - SFDR: 85 dBc (Except HD2, HD3, and Interleaving Tones)
- Channel Isolation: 100 dBc at fIN = 170 MHz
- Input Full-Scale: 1.9 VPP
- Input Bandwidth (3 dB): 1.2 GHz

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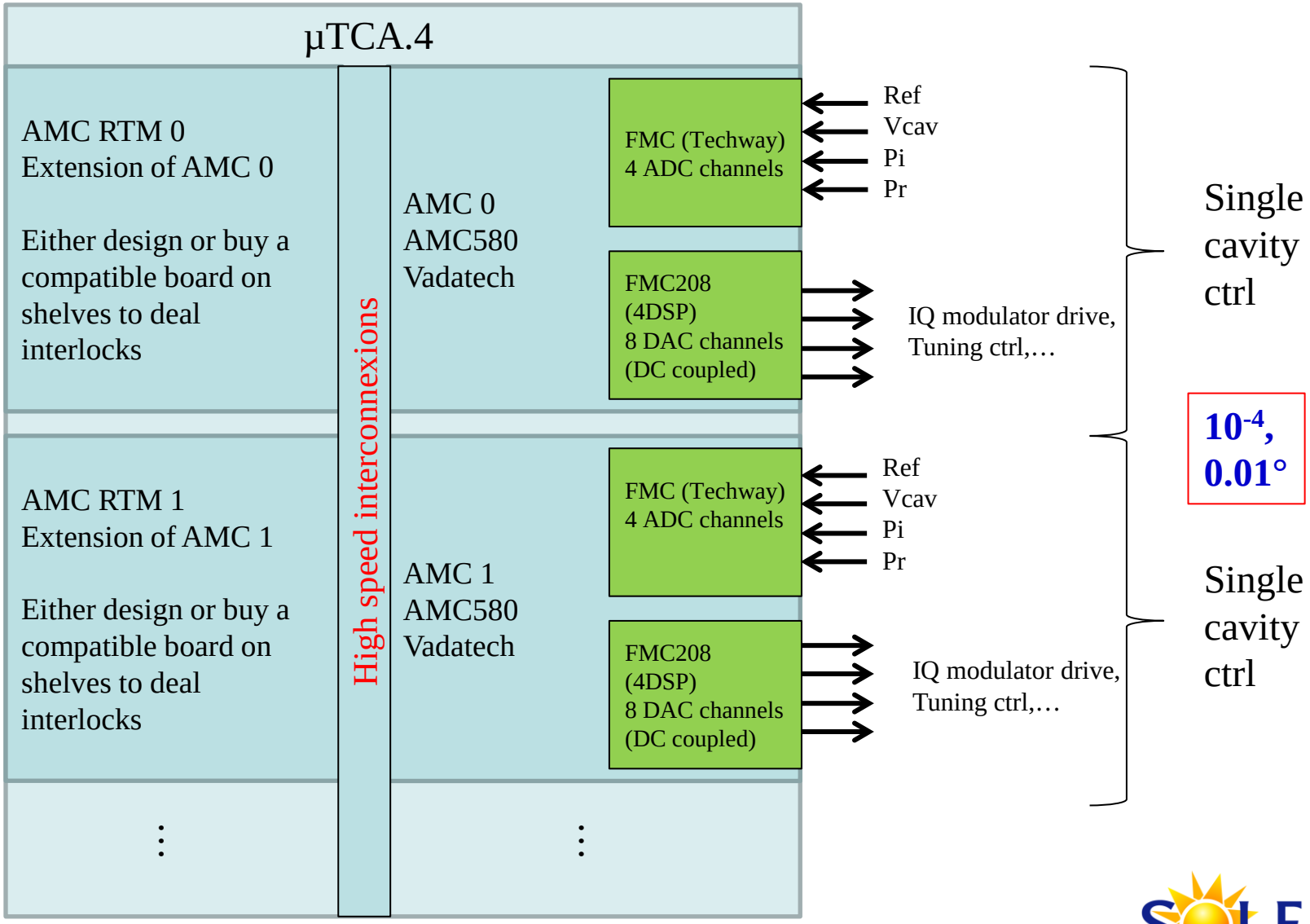
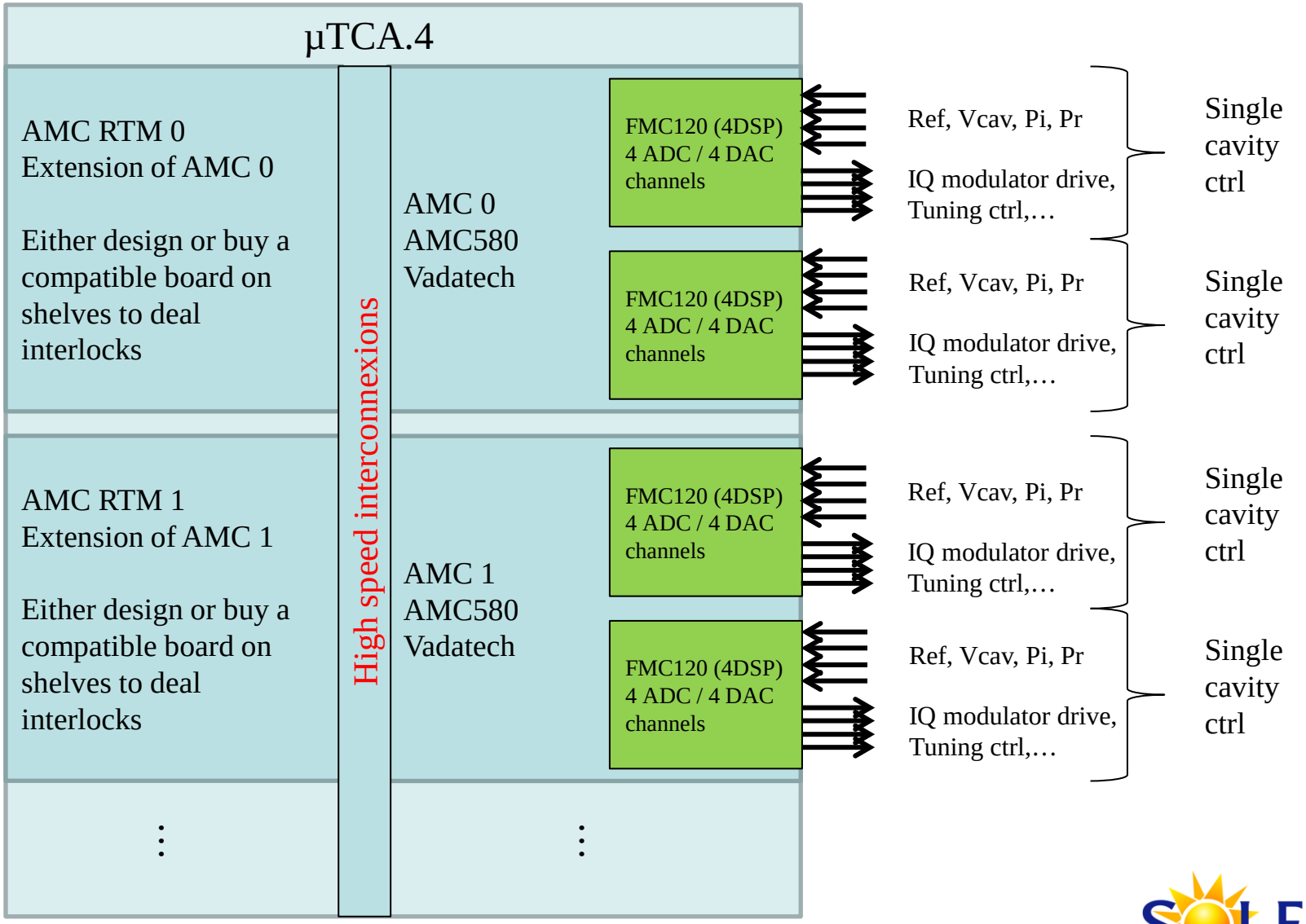
# Digital LLRF architecture for LUCRECE



# Digital LLRF architecture for Soleil RF upgrade




Relax on phase noise specifications and use FMC120.

# Conclusion

- Developments continue
- Have to be comfortable with µTCA-4, Zynq, JESD204B protocol
- Work to ensure the sustainability of systems and components
- Need for a good team work to reach quickly the goal

(+ external collaborations?)

Questions?